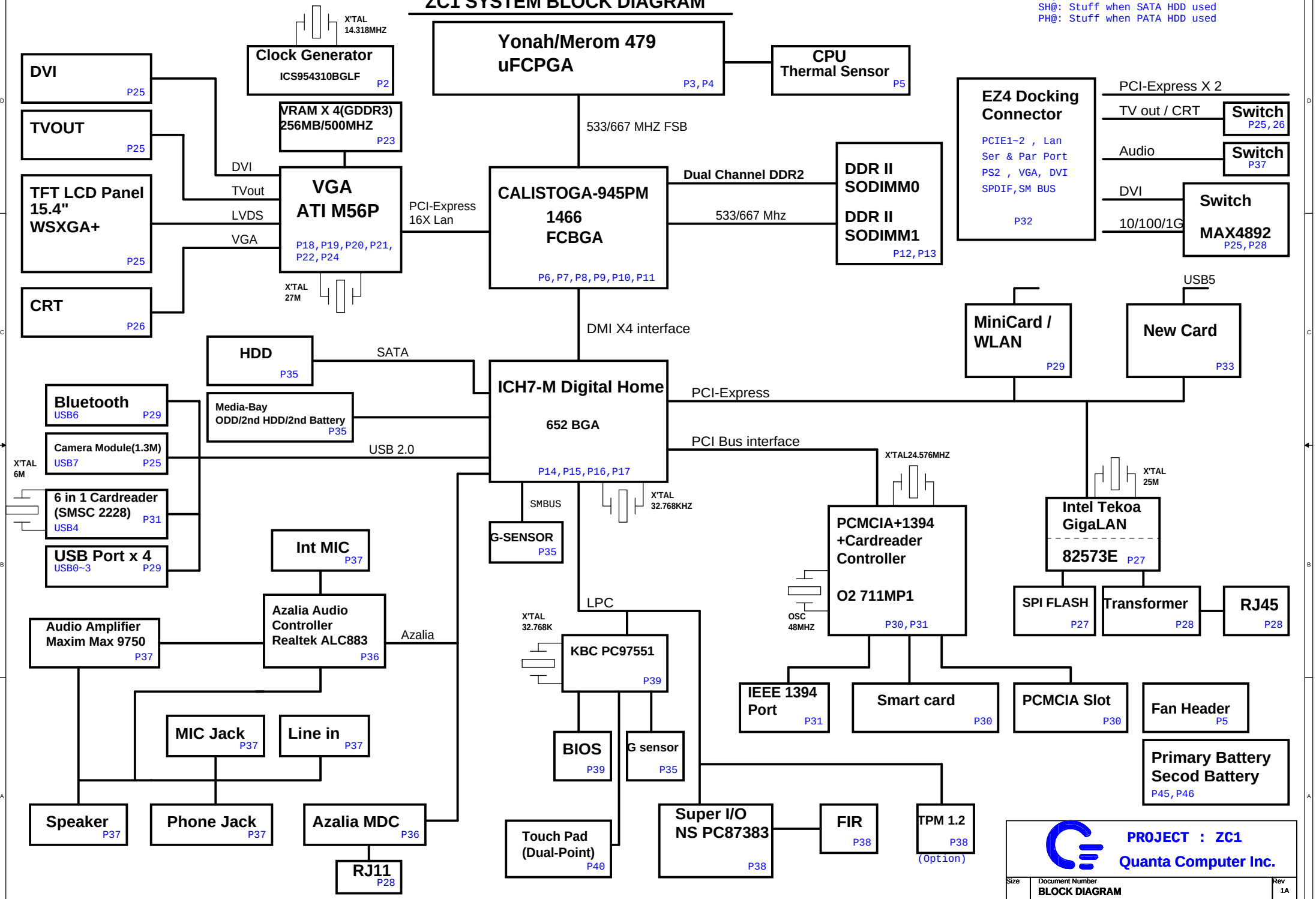
ZC1 SYSTEM BLOCK DIAGRAM

EV@: Stuff when external VGA used
SH@: Stuff when SATA HDD used
PH@: Stuff when PATA HDD used

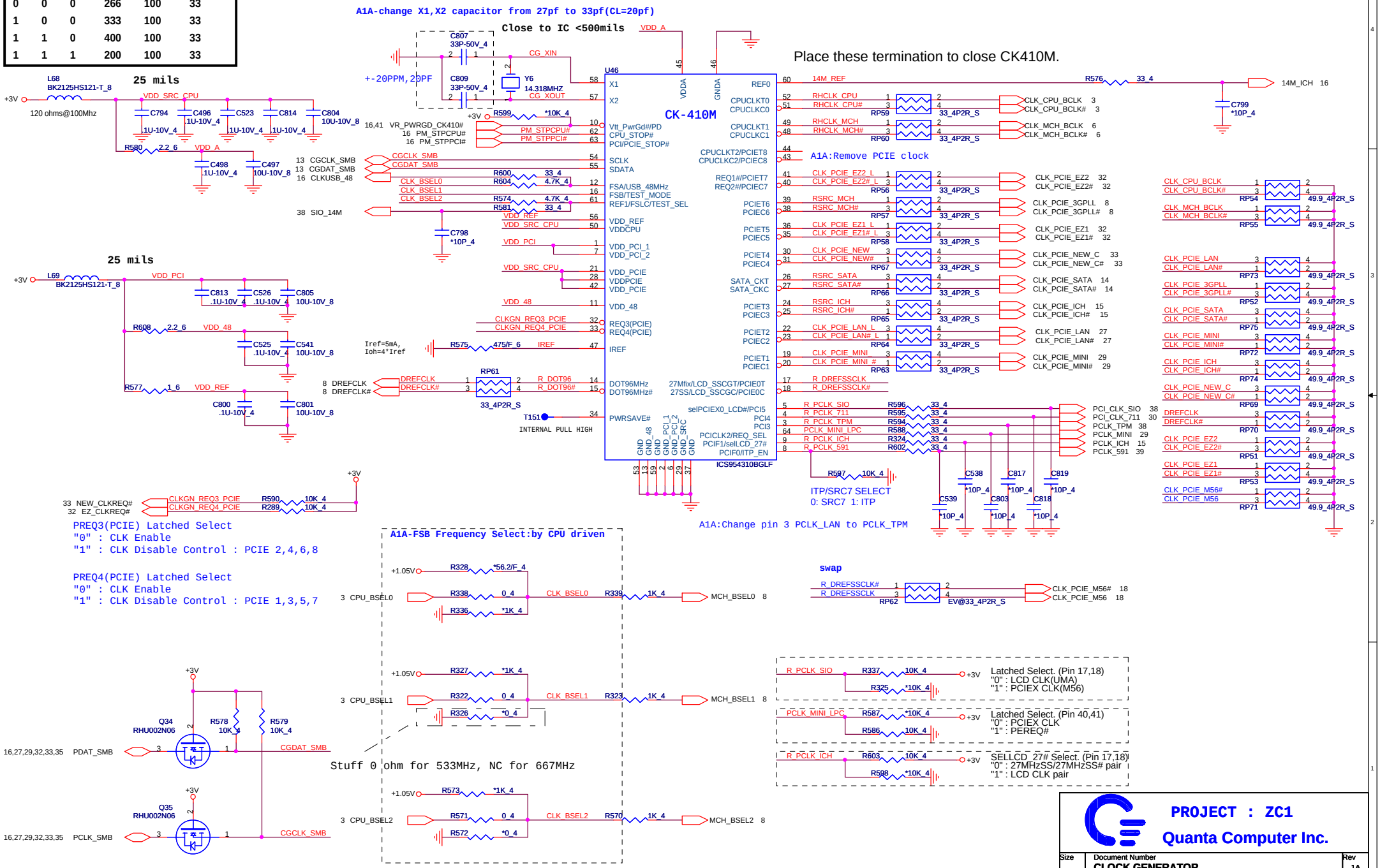


PROJECT : ZC1
Quanta Computer Inc.

Size	Document Number	Rev
	BLOCK DIAGRAM	1A

Date: Monday, November 07, 2005 Sheet 1 of 46

FSC	FSB	FSA	CPU	SRC	PCI	
1	0	1	100	100	33	
0	0	1	133	100	33	Default
0	1	1	166	100	33	
0	1	0	200	100	33	
0	0	0	266	100	33	
1	0	0	333	100	33	
1	1	0	400	100	33	
1	1	1	200	100	33	

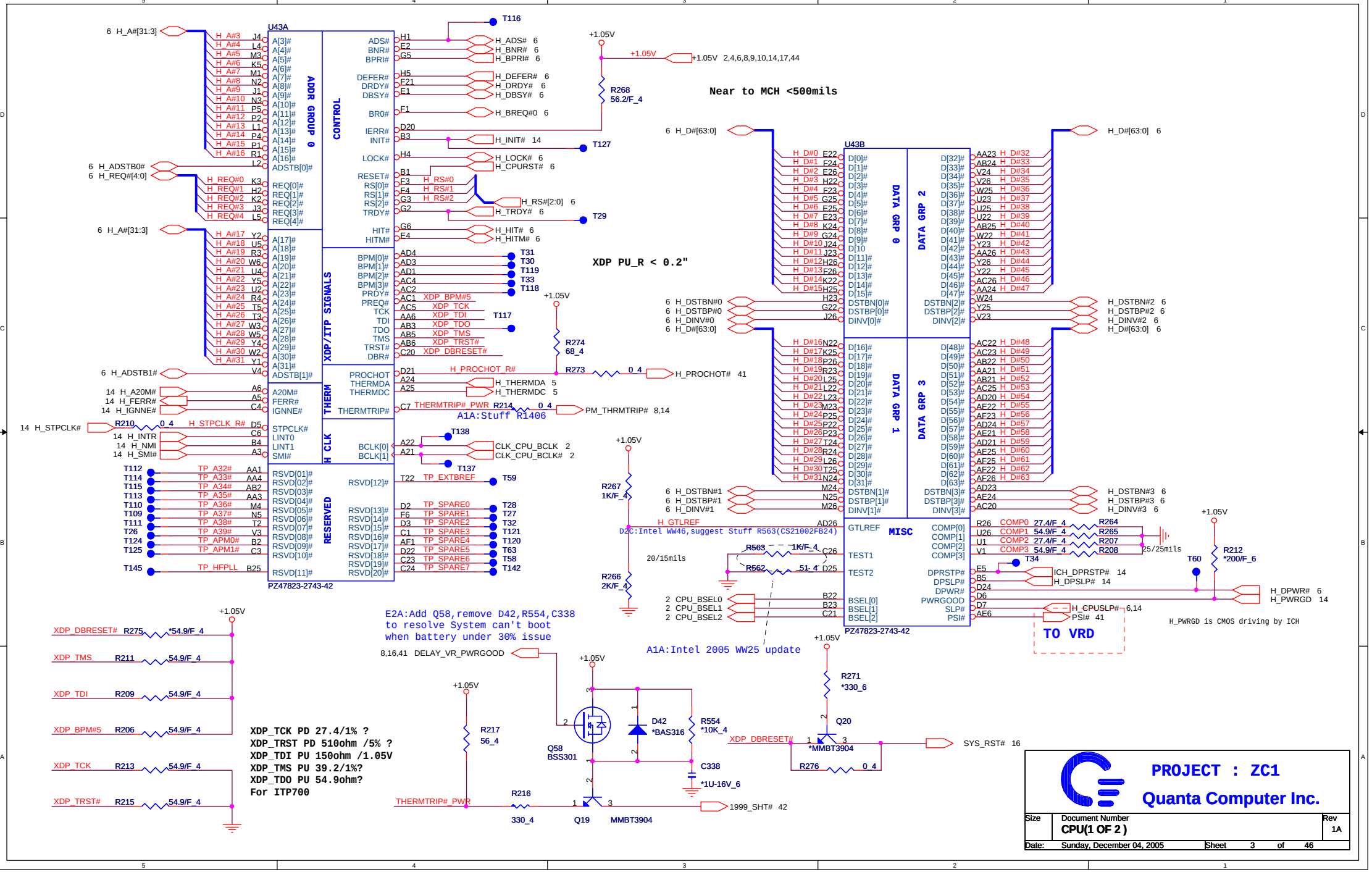


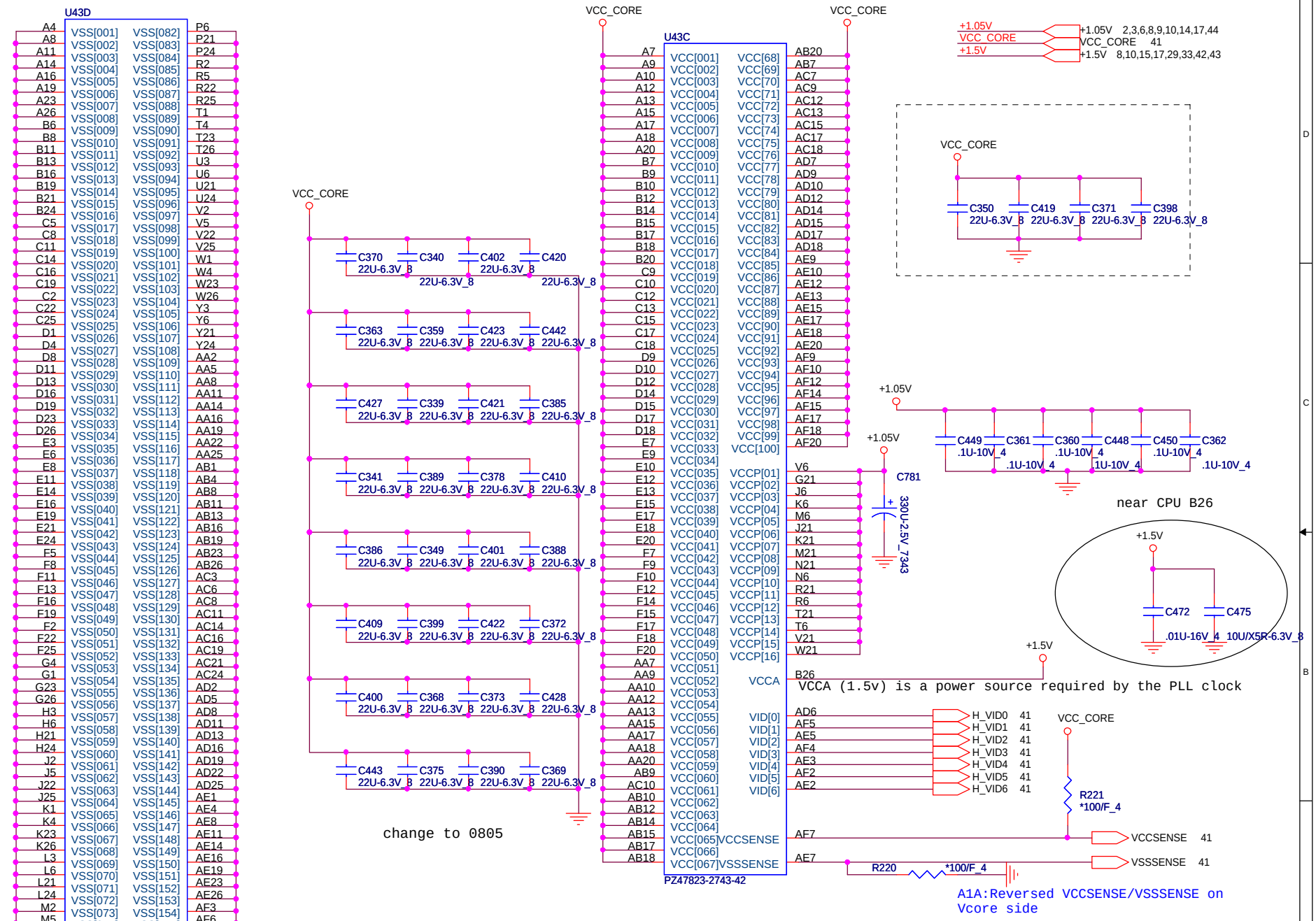
PROJECT : ZC1

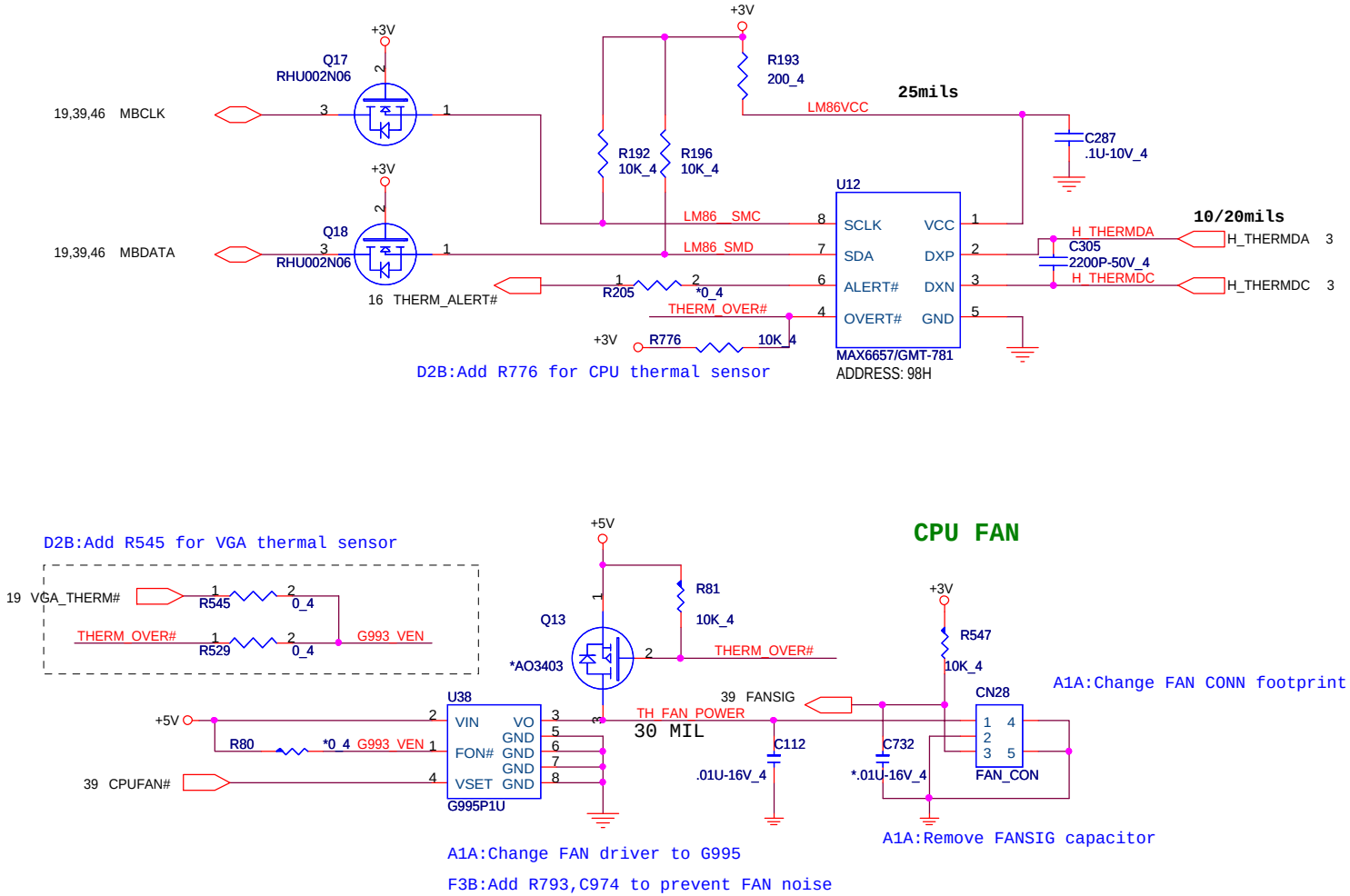
Quanta Computer Inc.

Size	Document Number	Rev
	CLOCK GENERATOR	1A

Date: Friday, December 09, 2005 Sheet 2 of 46


U43A
ADDR GROUP 0
CONTROL
XDP/ITP SIGNALS
THERM
H CLK
RESERVED
PZ47823-2743-42
U43B
DATA GRP 0
DATA GRP 1
DATA GRP 2
DATA GRP 3
MISC
PZ47823-2743-42
Near to MCH <500mils
XDP PU_R < 0.2"
A1A:Stuff R1406
D2C:Intel WW46,suggest Stuff R563(CS21002FB24)
E2A:Add Q58,remove D42,R554,C338
to resolve System can't boot
when battery under 30% issue
A1A:Intel 2005 WW25 update
TO VRD
H_PWRGD is CMOS driving by ICH
XDP_TCK PD 27.4/1% ?
XDP_TRST PD 510ohm /5% ?
XDP_TDI PU 150ohm /1.05V
XDP_TMS PU 39.2/1%?
XDP_TDO PU 54.9ohm?
For ITP700
PROJECT : ZC1
Quanta Computer Inc.
Size
Document Number
CPU(1 OF 2)
Rev
1A
Date: Sunday, December 04, 2005
Sheet 3 of 46


U43D
PZ47823-2743-42
U43C
PZ47823-2743-42
VCC_CORE
+1.05V
+1.5V
C350 22U-6.3V_8
C419 22U-6.3V_8
C371 22U-6.3V_8
C398 22U-6.3V_8
C449 .1U-10V_4
C361 .1U-10V_4
C360 .1U-10V_4
C448 .1U-10V_4
C450 .1U-10V_4
C362 .1U-10V_4
C781 330U-2.5V_7343
near CPU B26
C472 .01U-16V_4
C475 10U/X5R-6.3V_8
VCCA (1.5v) is a power source required by the PLL clock
R221 *100/F_4
R220 *100/F_4
VCCSENSE 41
VSSSENSE 41
A1A:Reversed VCCSENSE/VSSSENSE on Vcore side
change to 0805
PROJECT : ZC1
Quanta Computer Inc.
Size
Document Number
CPU(2 OF 2)
Rev
1A
Date: Monday, November 28, 2005
Sheet 4 of 46

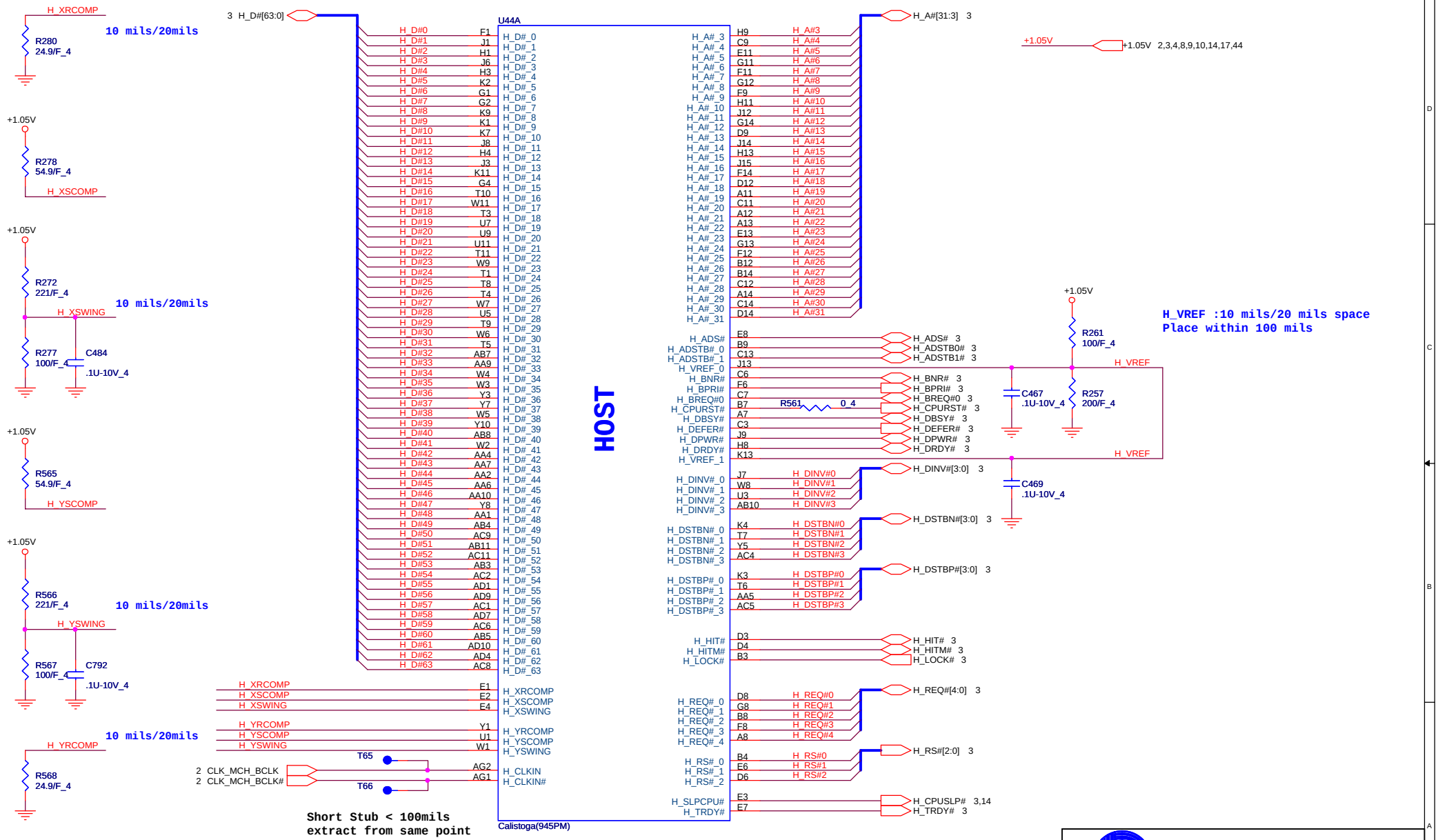


PROJECT : ZC1

Quanta Computer Inc.

Size	Document Number	Rev
	Thermal Sensor,FAN	1A

Date: Friday, December 02, 2005 Sheet 5 of 46

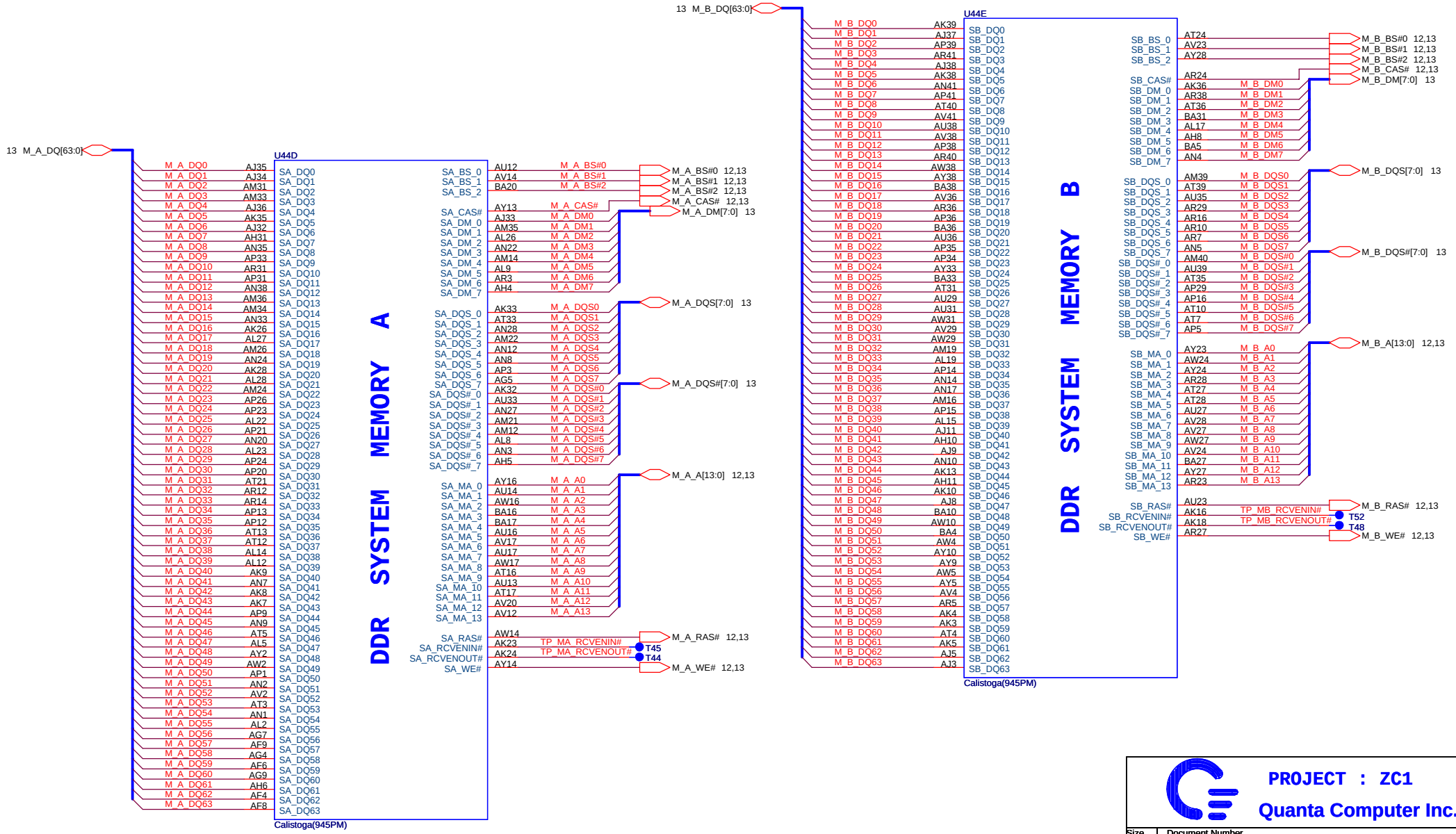


PROJECT : ZC1

Quanta Computer Inc.

Size	Document Number	Rev
	GMCH HOST(1 OF 6)	1A

Date: Friday, December 02, 2005 Sheet 6 of 46

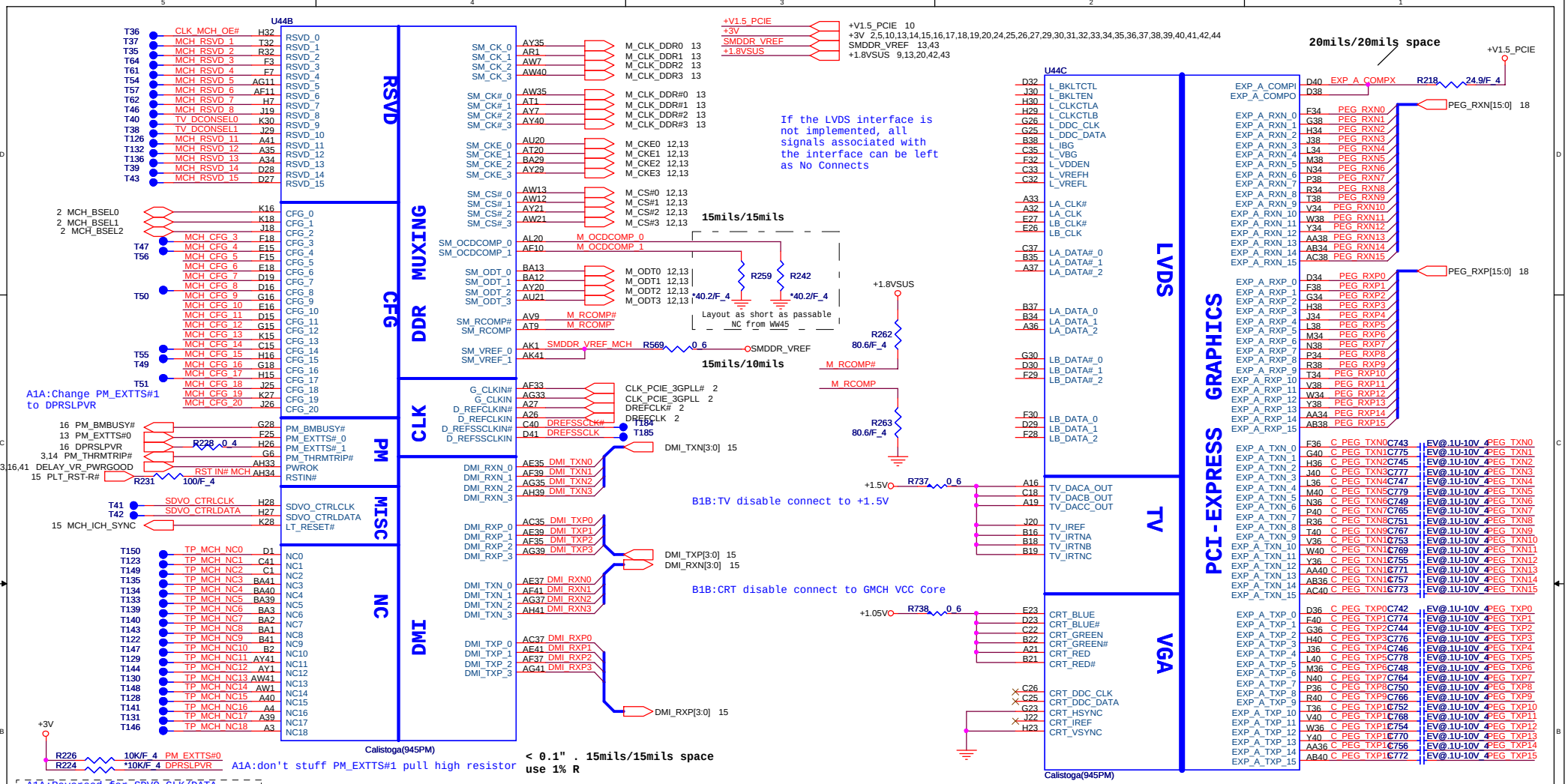


PROJECT : ZC1

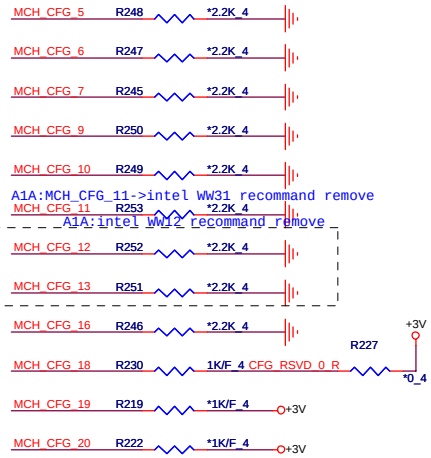
Quanta Computer Inc.

Size	Document Number	Rev
	GMCH DDR(2 OF 6)	1A

Date: Friday, December 02, 2005 Sheet 7 of 46



GMCH Strap pin



PULL LOW FOR DVO NOT PRESENT(INTERNAL PULLLOW IN 915GM)

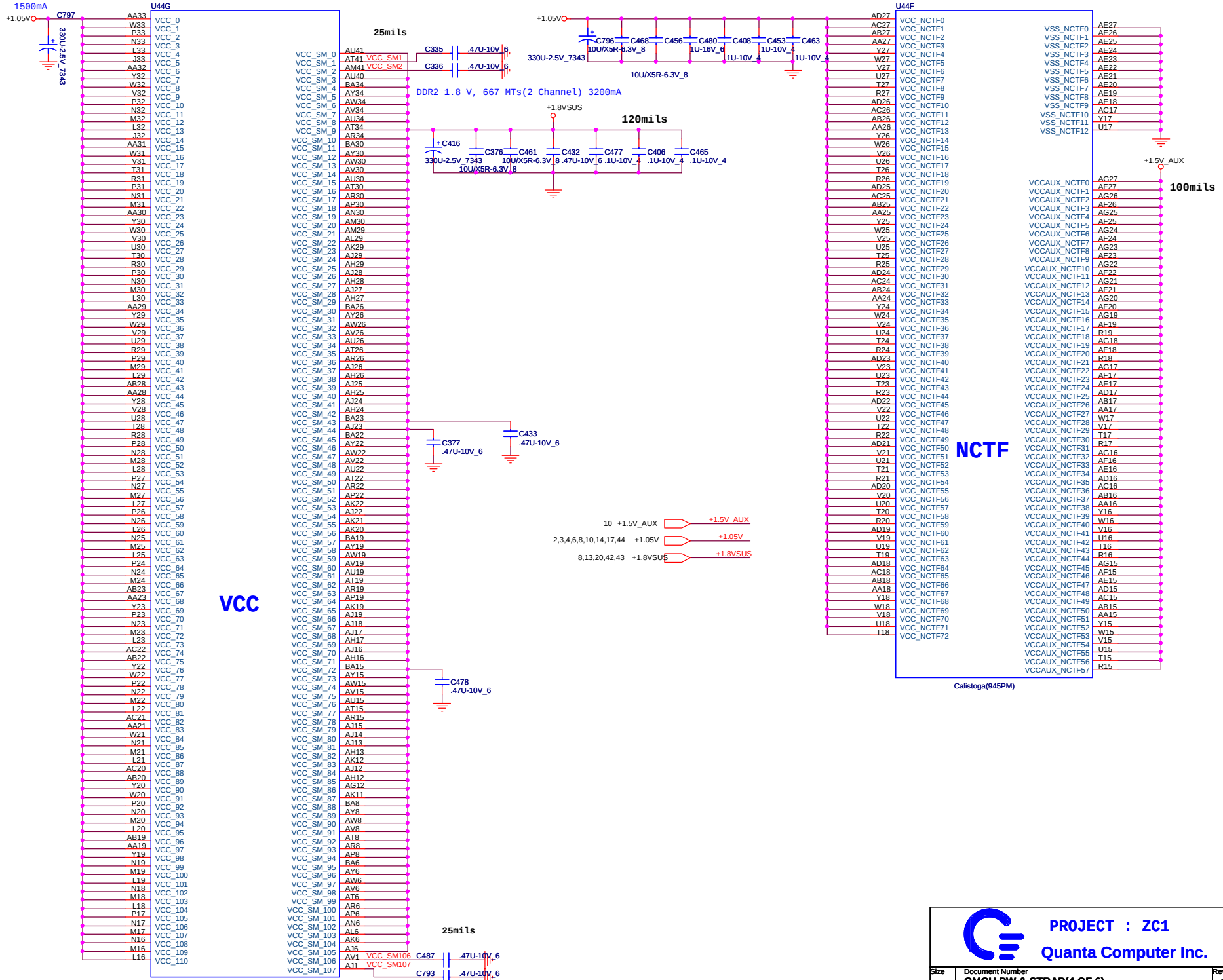
1. MCH_CFG_5 Low = DMI X2, High=DMIX4
2. MCH_CFG_6 DDR : Low =Moby Dick, High= Calistoga (Default)
3. MCH_CFG_7 CPU Strap Low=RSVD, High=Mobile CPU
4. MCH_CFG_9 PCI Exp Graphics Lane: Low =Reserved,High=Mobility
5. MCH_CFG_10 Host PLL VCC Select: Low=Reserved, High=Mobility
6. **MCH_CFG_11: PSB 4x CLK ENABLE Low=Reserved, High=Calistoga**
7. MCH_CFG_16 FSB Dynmic ODT: Low=Dynamic ODT Disabled, High=Dynamic ODT Enabled.
8. MCH_CFG_18 VCC Select: LOW=1.05V, High=1.5V
9. MCH_CFG_19 DMI LANE Reversal: Low=Normal,High=LANES Reversed.
10. MCH_CFG_20 PCIE Backward interpoerability mode: Low= only SDVO or PCIE x1 is operational (defaults) ,High=SDVO and PCIE x1 are operation simultaneously via the PEG port.

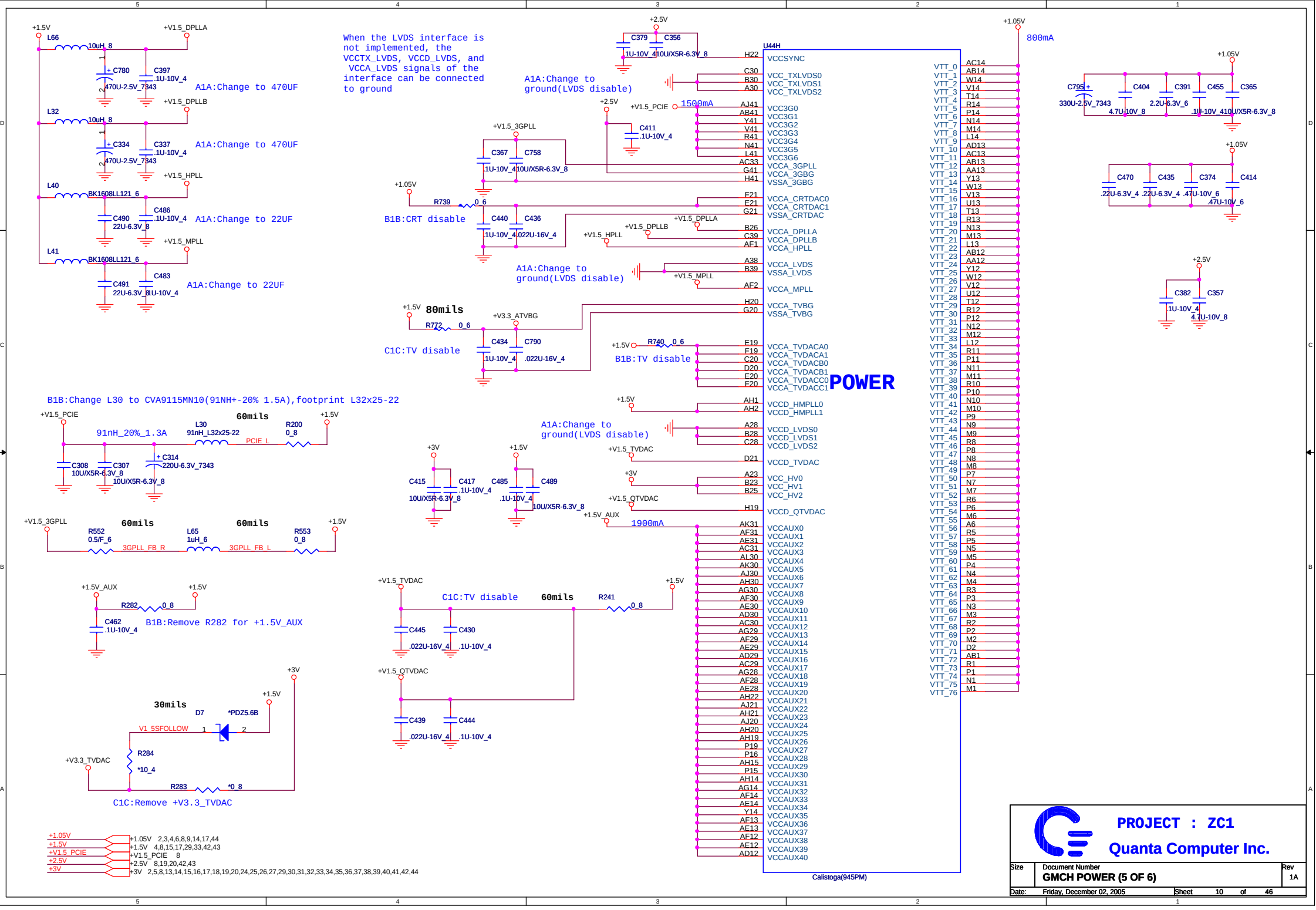
PROJECT : ZC1

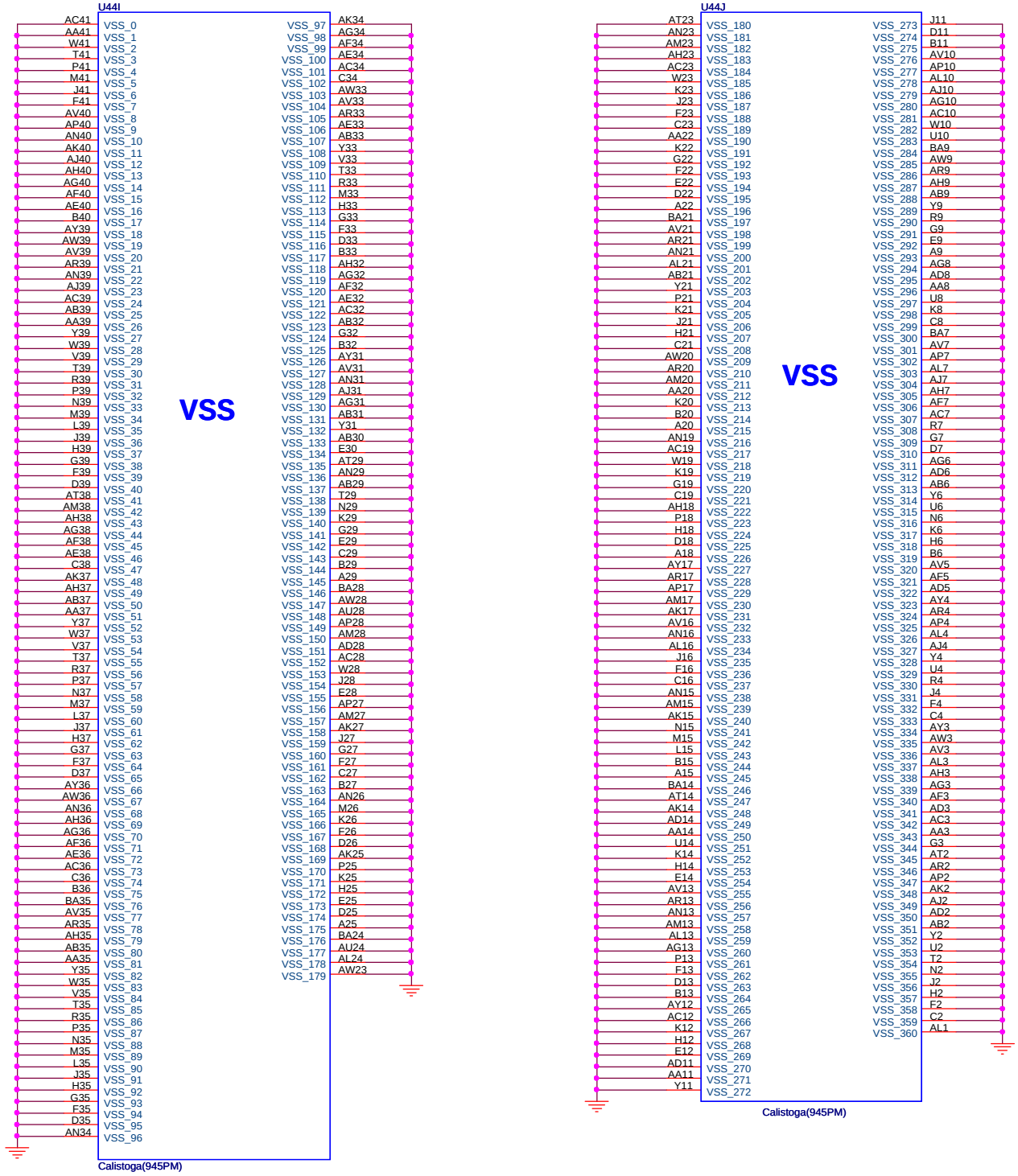
Quanta Computer Inc.

Size	Document Number	Rev
	GMCH DMI/VEDIO(3 OF 6)	1A

Date: Tuesday, December 06, 2005 Sheet 8 of 46


1500mA
+1.05V
C797
330U-2.5V_7343
U44G
VCC
Calistoga(945PM)
25mils
C335 .47U-10V_6
C336 .47U-10V_6
VCC_SM1
VCC_SM2
DDR2 1.8 V, 667 MTs(2 Channel) 3200mA
+1.8VSUS
120mils
C416
330U-2.5V_7343
C376 10U/X5R-6.3V_8
C461 10U/X5R-6.3V_8
C432 .47U-10V_6
C477 .1U-10V_4
C406 .1U-10V_4
C465 .1U-10V_4
C377 .47U-10V_6
C433 .47U-10V_6
C478 .47U-10V_6
C487 .47U-10V_6
C793 .47U-10V_6
VCC_SM106
VCC_SM107
+1.05V
C796 10U/X5R-6.3V_8
C468 10U/X5R-6.3V_8
C456 10U/X5R-6.3V_8
C480 1U-16V_6
C408 .1U-10V_4
C453 .1U-10V_4
C463 .1U-10V_4
330U-2.5V_7343
U44F
NCTF
Calistoga(945PM)
+1.5V_AUX
100mils
10 +1.5V_AUX
2,3,4,6,8,10,14,17,44 +1.05V
8,13,20,42,43 +1.8VSUS
PROJECT : ZC1
Quanta Computer Inc.
Size
Document Number
GMCH PW & STRAP(4 OF 6)
Rev
1A
Date: Friday, December 02, 2005
Sheet 9 of 46


When the LVDS interface is not implemented, the VCCTX_LVDS, VCCD_LVDS, and VCCA_LVDS signals of the interface can be connected to ground
A1A:Change to 470UF
A1A:Change to 470UF
A1A:Change to 22UF
A1A:Change to 22UF
A1A:Change to ground(LVDS disable)
B1B:CRT disable
A1A:Change to ground(LVDS disable)
80mils
C1C:TV disable
B1B:TV disable
B1B:Change L30 to CVA9115MN10(91NH+-20% 1.5A),footprint L32x25-22
60mils
91nH_20%_1.3A
A1A:Change to ground(LVDS disable)
60mils
60mils
B1B:Remove R282 for +1.5V_AUX
C1C:TV disable
60mils
30mils
C1C:Remove +V3.3_TVDAC
U44H
POWER
Calistoga(945PM)
800mA
1500mA
1900mA
+1.05V 2,3,4,6,8,9,14,17,44
+1.5V 4,8,15,17,29,33,42,43
+V1.5_PCIE 8
+2.5V 8,19,20,42,43
+3V 2,5,8,13,14,15,16,17,18,19,20,24,25,26,27,29,30,31,32,33,34,35,36,37,38,39,40,41,42,44
PROJECT : ZC1
Quanta Computer Inc.
Size
Document Number
GMCH POWER (5 OF 6)
Rev
1A
Date: Friday, December 02, 2005
Sheet 10 of 46



PROJECT : ZC1

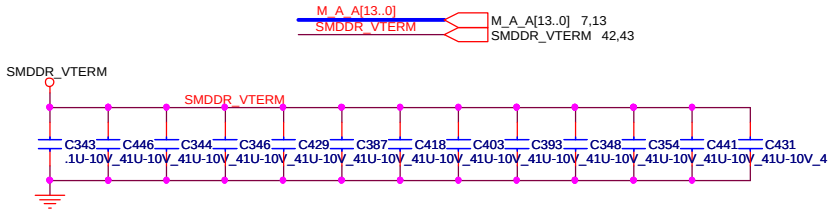
Quanta Computer Inc.

Size	Document Number	Rev
	GMCH GND(6 OF 6)	1A

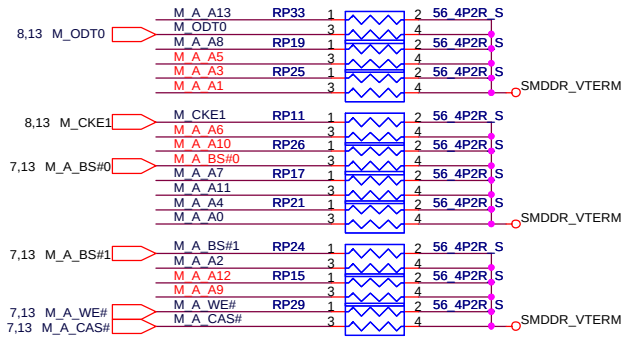
Date: Friday, December 02, 2005 Sheet 11 of 46

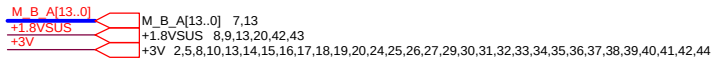
DDRII DUAL CHANNEL A,B.

DDRII A CHANNEL

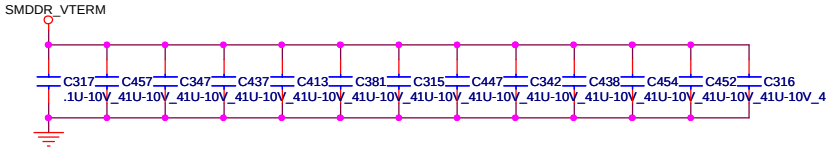


A1A:Swap net



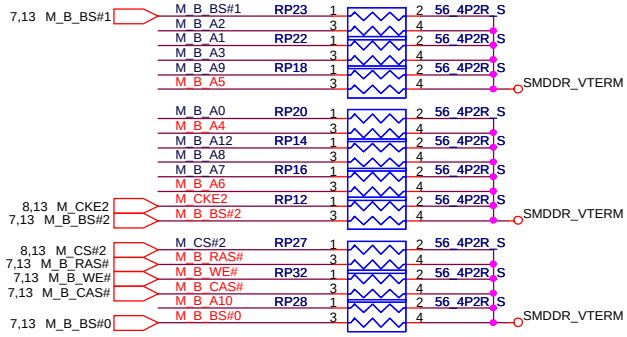


DDRII B CHANNEL

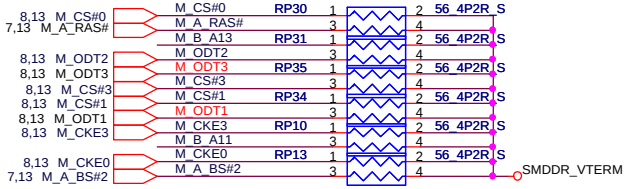


Layout note: Place one cap close to every 2 pullup resistors terminated to SMDDR_VTERM

A1A:Swap net



A1A:Swap net



PROJECT : ZC1

Quanta Computer Inc.

Size	Document Number	Rev
	DDR RES. ARRAY	1A

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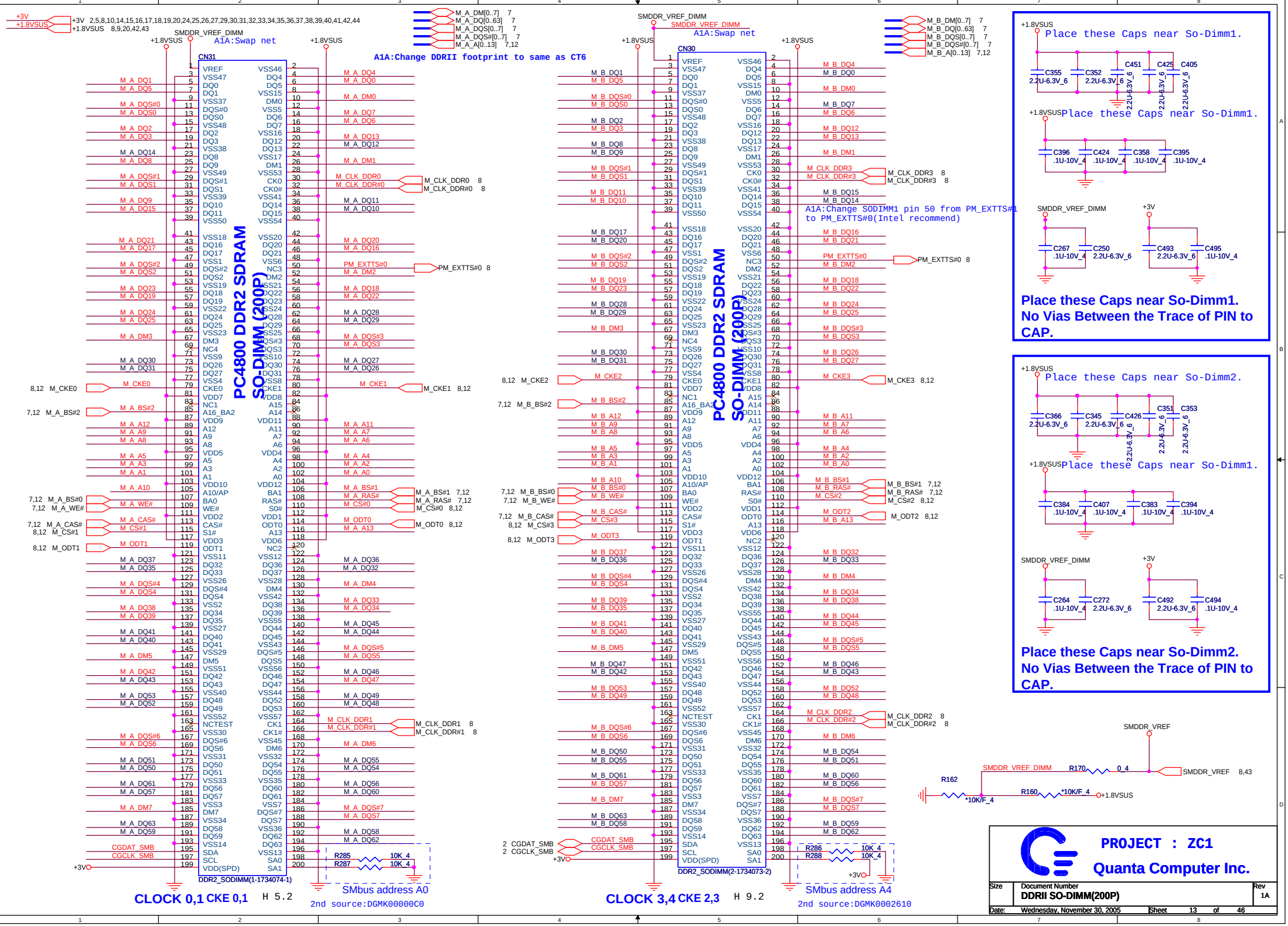

CN31
PC4800 DDR2 SDRAM
SO-DIMM (200P)
DDR2_SODIMM(1-1734074-1)
A1A:Swap net
A1A:Change DDRII footprint to same as CT6
SMDDR_VREF_DIMM
+1.8VSUS
+3V
CLOCK 0,1 CKE 0,1
H 5.2
SMbus address A0
2nd source:DGMK00000C0
CN30
DDR2_SODIMM(2-1734073-2)
A1A:Change SODIMM1 pin 50 from PM_EXTTS#1 to PM_EXTTS#0(Intel recommend)
CLOCK 3,4 CKE 2,3
H 9.2
SMbus address A4
2nd source:DGMK0002610
Place these Caps near So-Dimm1.
Place these Caps near So-Dimm1.
Place these Caps near So-Dimm1.
No Vias Between the Trace of PIN to CAP.
Place these Caps near So-Dimm2.
Place these Caps near So-Dimm2.
Place these Caps near So-Dimm2.
No Vias Between the Trace of PIN to CAP.
SMDDR_VREF
R162
R170
R160
PROJECT : ZC1
Quanta Computer Inc.
Size
Document Number
DDRII SO-DIMM(200P)
Rev
1A
Date: Wednesday, November 30, 2005
Sheet 13 of 46

RTC

CKL:C1/C2: 18pF -> CL:12.5pF
C1/C: 10pF -> CL Value = 8.5pF
A1A:Change RTXC1/RTXC2 from 10pf to 18pf

A1A:Change RTC Connector footprint

B1B:Per Intel Comment,don't stuff R307 for CPUSLP#

Should be 2" close ICH7

A series termination resistor is required for the PRIMARY CODEC

B1B:Add R719 for BIT_CLK_MODEM

ICH7 internal VR enable strap

	INTVRMEN
Enable (default)	1
Disable	0

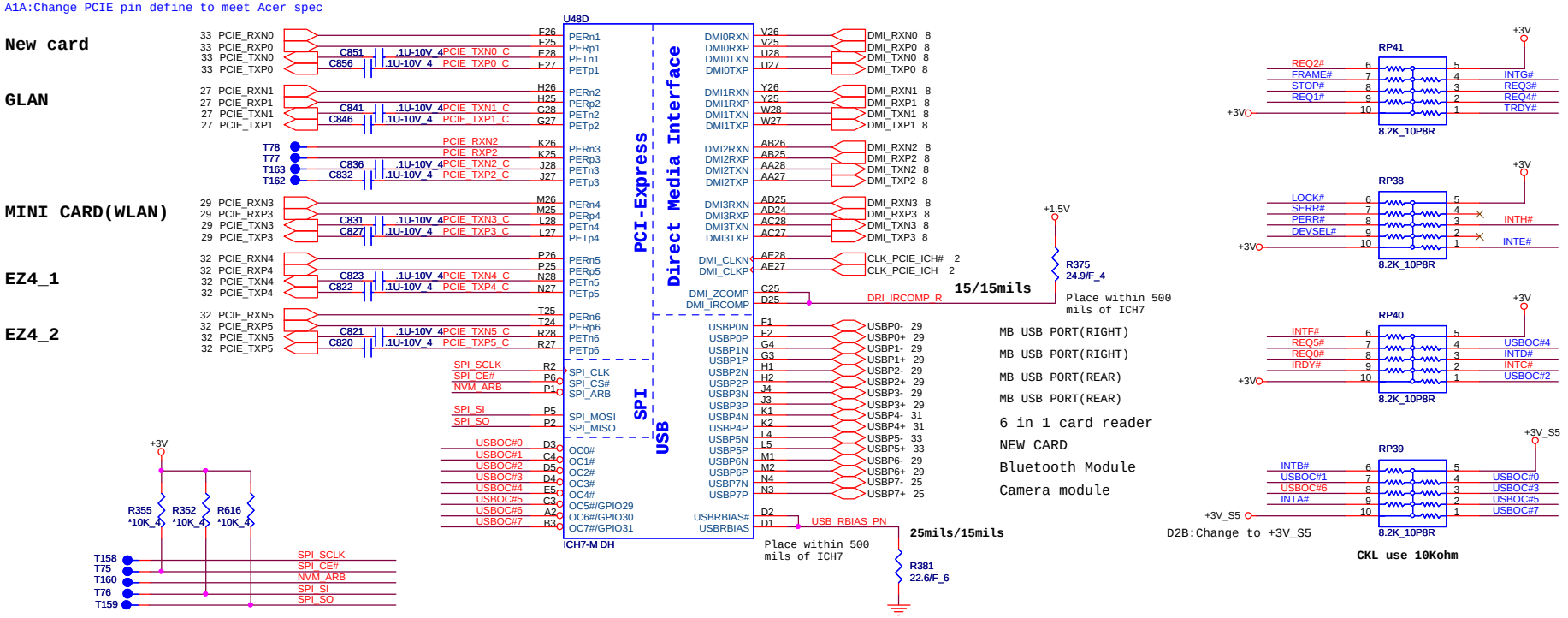
PROJECT : ZC1

Quanta Computer Inc.

Size	Document Number	Rev
	ICH7-M HOST (1 OF 4)	1A

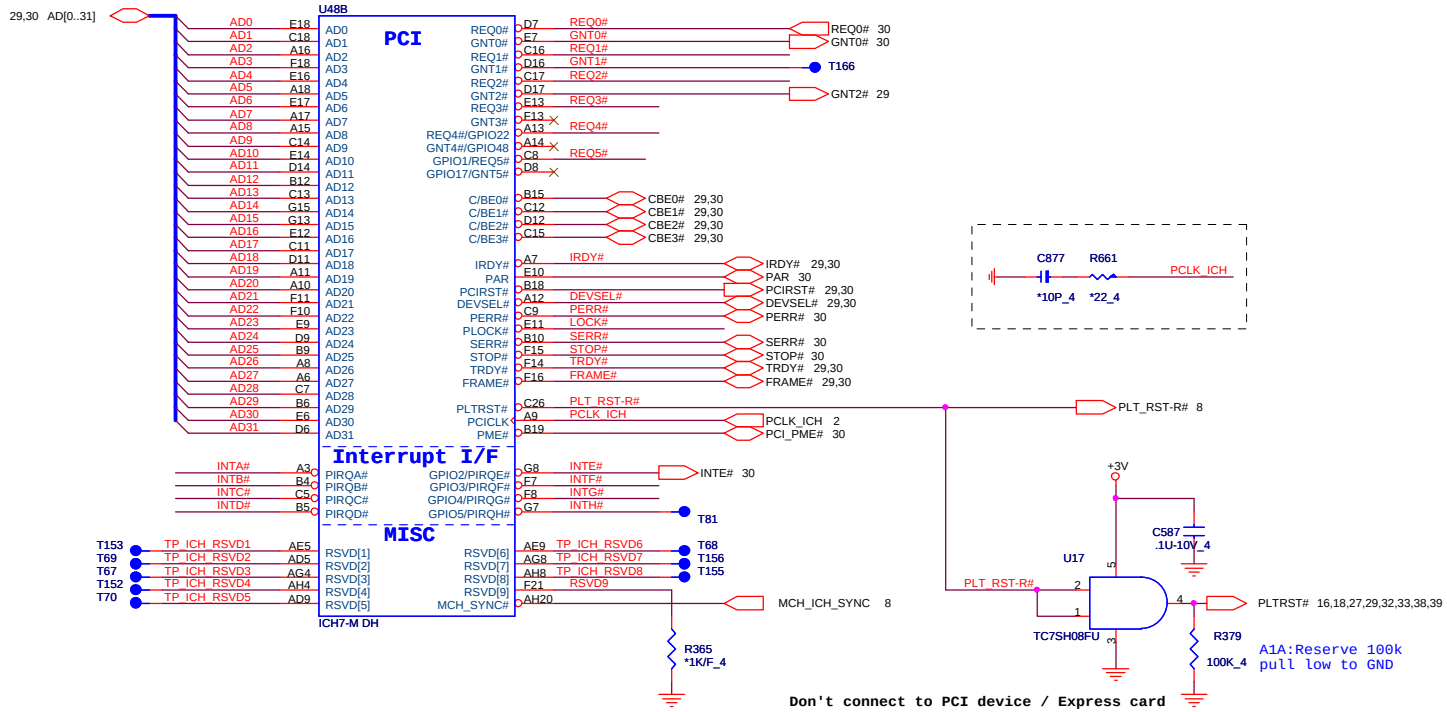
Date: Friday, December 02, 2005 Sheet 14 of 46

A1A:Change PCIE pin define to meet Acer spec



ICH7 Boot BIOS select

	STRAP	GNT5# R1	GNT4# R2
LPC (default)	11	UNSTUFF	UNSTUFF
PCI	10	UNSTUFF	STUFF
SPI	01	STUFF	UNSTUFF



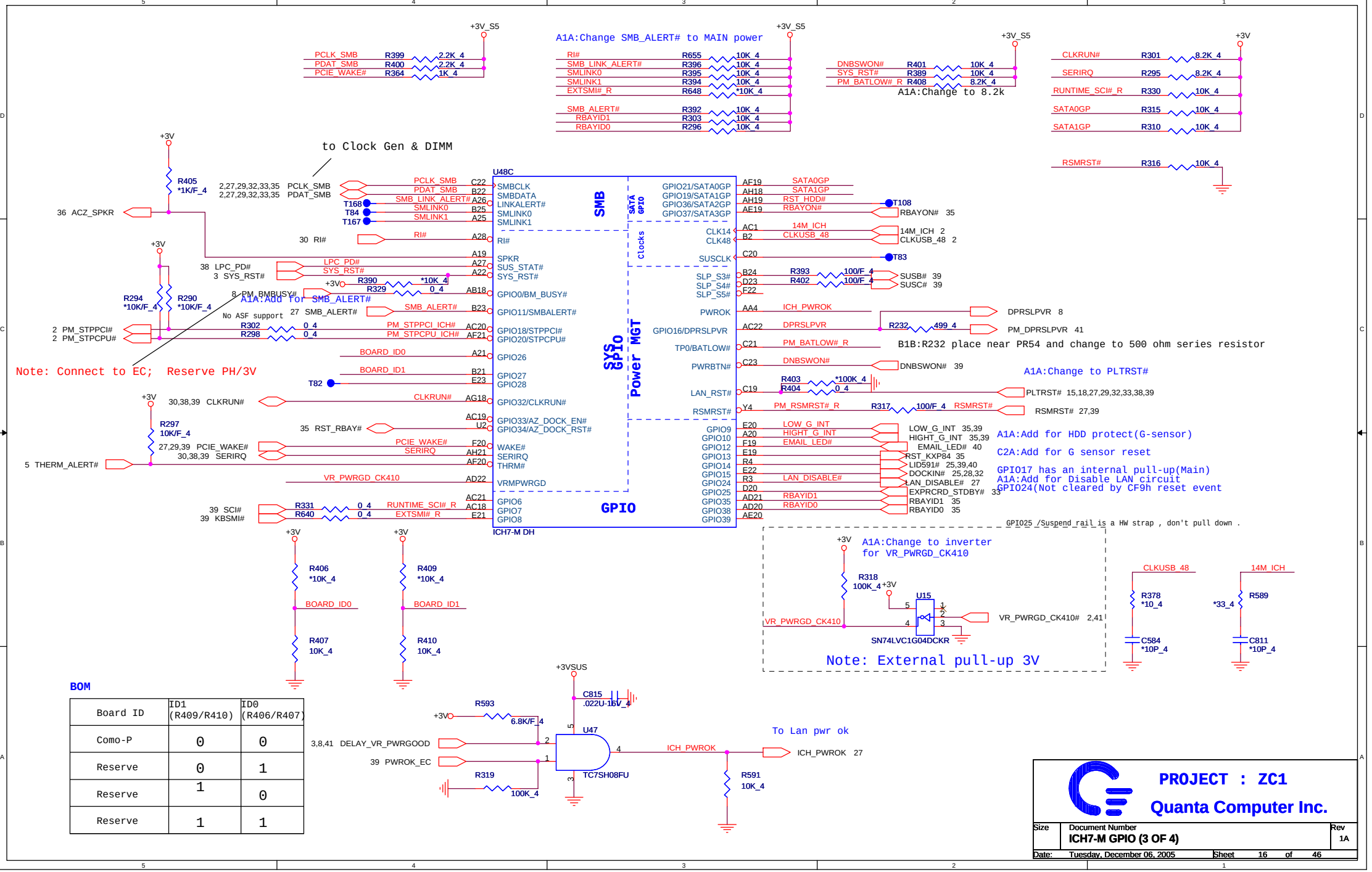
PCI DEVICE	IDSEL#	REQ# / GNT#	Interrupts
OZ711MP1	AD25	REQ0# / GNT0#	INTE#

PROJECT : ZC1

Quanta Computer Inc.

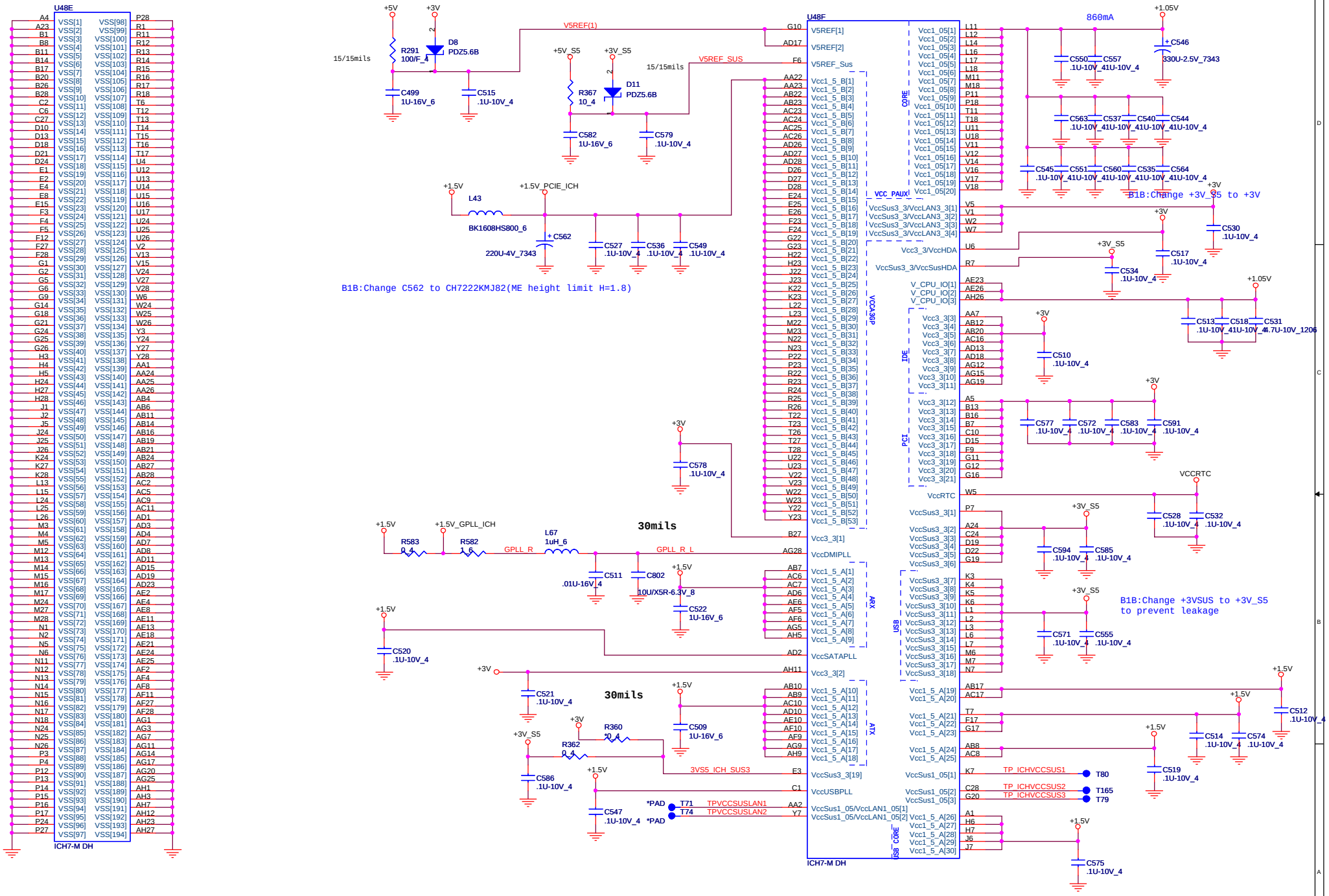
Size	Document Number	Rev
	ICH7-M PCI E (2 OF 4)	1A

Date: Friday, December 09, 2005 Sheet 15 of 46



BOM

Board ID	ID1 (R409/R410)	ID0 (R406/R407)
Como-P	0	0
Reserve	0	1
Reserve	1	0
Reserve	1	1


U48E
ICH7-M DH
U48F
ICH7-M DH
V5REF(1)
V5REF_SUS
15/15mils
R291 100/F_4
D8 PDZ5.6B
D11 PDZ5.6B
R367 10_4
C499 1U-16V_6
C515 .1U-10V_4
C582 1U-16V_6
C579 .1U-10V_4
L43
BK1608HS800_6
C562 220U-4V_7343
C527 .1U-10V_4
C536 .1U-10V_4
C549 .1U-10V_4
B1B:Change C562 to CH7222KMJ82(ME height limit H=1.8)
C578 .1U-10V_4
R583 0_4
R582 1_6
L67 1uH_6
GPLL_R
GPLL_R_L
30mils
C511 .01U-16V_4
C802 10U/X5R-6.3V_8
C522 1U-16V_6
C520 .1U-10V_4
C521 .1U-10V_4
R360 20_4
R362 0_4
C509 1U-16V_6
C586 .1U-10V_4
3VS5_ICH_SUS3
C547 .1U-10V_4
T71 TPVCCSUSLAN1
T74 TPVCCSUSLAN2
860mA
C546 330U-2.5V_7343
B1B:Change +3V_S5 to +3V
C530 .1U-10V_4
C517 .1U-10V_4
C534 .1U-10V_4
C513 .1U-10V_4
C518 .1U-10V_4
C531 4.7U-10V_1206
C510 .1U-10V_4
C577 .1U-10V_4
C572 .1U-10V_4
C583 .1U-10V_4
C591 .1U-10V_4
C528 .1U-10V_4
C532 .1U-10V_4
C594 .1U-10V_4
C585 .1U-10V_4
B1B:Change +3VSUS to +3V_S5 to prevent leakage
C571 .1U-10V_4
C555 .1U-10V_4
C512 .1U-10V_4
C514 .1U-10V_4
C574 .1U-10V_4
C519 .1U-10V_4
TP_ICHVCCSUS1 T80
TP_ICHVCCSUS2 T165
TP_ICHVCCSUS3 T79
C575 .1U-10V_4
PROJECT : ZC1
Quanta Computer Inc.
Size
Document Number
ICH7-M POWER (4 OF 4)
Rev 1A
Date: Friday, December 02, 2005
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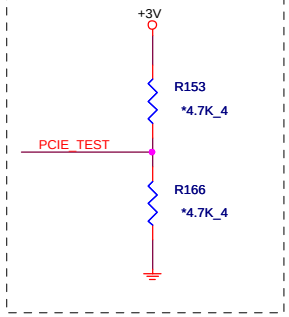
PCIE TEST PADS
PCIE TEST POINTS MUST BE WITHIN 250 MILS
OF THE ASIC BALL WITH POSITIVE AND NEGATIVE
SIGNALS THE SAME DISTANCE

8 PEG_RXP[15:0]
8 PEG_RXN[15:0]
8 PEG_TXP[15:0]
8 PEG_TXN[15:0]

ATI FEATURE NOT ENABLED (M52P,M54P,M56P)
B1B:Don't stuff R153,R166 for PCIE_TEST



U41A

PART 1 OF 7

PCI-EXPRESS INTERFACE

PEG_TXP0	AJ31	PCIE_RX0P	PCIE_TX0P	AK27	V_GMCHEXP_RXP0	C304	EV@.1U-10V_4 PEG_RXP0
PEG_TXN0	AH31	PCIE_RX0N	PCIE_TX0N	AJ27	V_GMCHEXP_RXN0	C303	EV@.1U-10V_4 PEG_RXN0
PEG_TXP1	AH30	PCIE_RX1P	PCIE_TX1P	AJ25	V_GMCHEXP_RXP1	C333	EV@.1U-10V_4 PEG_RXP1
PEG_TXN1	AG30	PCIE_RX1N	PCIE_TX1N	AH25	V_GMCHEXP_RXN1	C332	EV@.1U-10V_4 PEG_RXN1
PEG_TXP2	AG32	PCIE_RX2P	PCIE_TX2P	AH28	V_GMCHEXP_RXP2	C302	EV@.1U-10V_4 PEG_RXP2
PEG_TXN2	AF32	PCIE_RX2N	PCIE_TX2N	AG28	V_GMCHEXP_RXN2	C301	EV@.1U-10V_4 PEG_RXN2
PEG_TXP3	AF31	PCIE_RX3P	PCIE_TX3P	AG27	V_GMCHEXP_RXP3	C331	EV@.1U-10V_4 PEG_RXP3
PEG_TXN3	AE31	PCIE_RX3N	PCIE_TX3N	AF27	V_GMCHEXP_RXN3	C330	EV@.1U-10V_4 PEG_RXN3
PEG_TXP4	AE30	PCIE_RX4P	PCIE_TX4P	AF25	V_GMCHEXP_RXP4	C300	EV@.1U-10V_4 PEG_RXP4
PEG_TXN4	AD30	PCIE_RX4N	PCIE_TX4N	AE25	V_GMCHEXP_RXN4	C299	EV@.1U-10V_4 PEG_RXN4
PEG_TXP5	AD32	PCIE_RX5P	PCIE_TX5P	AE28	V_GMCHEXP_RXP5	C329	EV@.1U-10V_4 PEG_RXP5
PEG_TXN5	AC32	PCIE_RX5N	PCIE_TX5N	AD28	V_GMCHEXP_RXN5	C328	EV@.1U-10V_4 PEG_RXN5
PEG_TXP6	AC31	PCIE_RX6P	PCIE_TX6P	AD27	V_GMCHEXP_RXP6	C298	EV@.1U-10V_4 PEG_RXP6
PEG_TXN6	AB31	PCIE_RX6N	PCIE_TX6N	AC27	V_GMCHEXP_RXN6	C297	EV@.1U-10V_4 PEG_RXN6
PEG_TXP7	AB30	PCIE_RX7P	PCIE_TX7P	AC25	V_GMCHEXP_RXP7	C327	EV@.1U-10V_4 PEG_RXP7
PEG_TXN7	AA30	PCIE_RX7N	PCIE_TX7N	AB25	V_GMCHEXP_RXN7	C326	EV@.1U-10V_4 PEG_RXN7
PEG_TXP8	AA32	PCIE_RX8P	PCIE_TX8P	AB28	V_GMCHEXP_RXP8	C296	EV@.1U-10V_4 PEG_RXP8
PEG_TXN8	Y32	PCIE_RX8N	PCIE_TX8N	AA28	V_GMCHEXP_RXN8	C295	EV@.1U-10V_4 PEG_RXN8
PEG_TXP9	Y31	PCIE_RX9P	PCIE_TX9P	AA27	V_GMCHEXP_RXP9	C325	EV@.1U-10V_4 PEG_RXP9
PEG_TXN9	W31	PCIE_RX9N	PCIE_TX9N	Y27	V_GMCHEXP_RXN9	C324	EV@.1U-10V_4 PEG_RXN9
PEG_TXP10	W30	PCIE_RX10P	PCIE_TX10P	Y25	V_GMCHEXP_RXP10	C294	EV@.1U-10V_4 PEG_RXP10
PEG_TXN10	V30	PCIE_RX10N	PCIE_TX10N	W25	V_GMCHEXP_RXN10	C293	EV@.1U-10V_4 PEG_RXN10
PEG_TXP11	V32	PCIE_RX11P	PCIE_TX11P	W28	V_GMCHEXP_RXP11	C323	EV@.1U-10V_4 PEG_RXP11
PEG_TXN11	U32	PCIE_RX11N	PCIE_TX11N	V28	V_GMCHEXP_RXN11	C322	EV@.1U-10V_4 PEG_RXN11
PEG_TXP12	U31	PCIE_RX12P	PCIE_TX12P	V27	V_GMCHEXP_RXP12	C292	EV@.1U-10V_4 PEG_RXP12
PEG_TXN12	T31	PCIE_RX12N	PCIE_TX12N	U27	V_GMCHEXP_RXN12	C291	EV@.1U-10V_4 PEG_RXN12
PEG_TXP13	T30	PCIE_RX13P	PCIE_TX13P	U25	V_GMCHEXP_RXP13	C321	EV@.1U-10V_4 PEG_RXP13
PEG_TXN13	R30	PCIE_RX13N	PCIE_TX13N	T25	V_GMCHEXP_RXN13	C320	EV@.1U-10V_4 PEG_RXN13
PEG_TXP14	R32	PCIE_RX14P	PCIE_TX14P	T28	V_GMCHEXP_RXP14	C290	EV@.1U-10V_4 PEG_RXP14
PEG_TXN14	P32	PCIE_RX14N	PCIE_TX14N	R28	V_GMCHEXP_RXN14	C289	EV@.1U-10V_4 PEG_RXN14
PEG_TXP15	P31	PCIE_RX15P	PCIE_TX15P	R27	V_GMCHEXP_RXP15	C319	EV@.1U-10V_4 PEG_RXP15
PEG_TXN15	N31	PCIE_RX15N	PCIE_TX15N	P27	V_GMCHEXP_RXN15	C318	EV@.1U-10V_4 PEG_RXN15

Clock

AL28	PCIE_REFCLKP	2 CLK_PCIE_M56
AK28	PCIE_REFCLKN	2 CLK_PCIE_M56#
AG24	PERSTB	PLTRST# M56
AA24	PCIE_TEST	PCIE_TEST
AF24	PERSTB_MASK	Tie To VSS

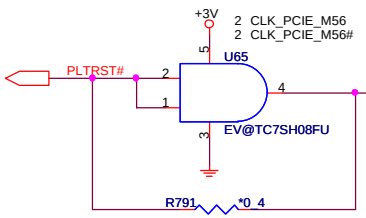
Calibration

AE24	PCIE_CALRN	R156	EV@2K/F_4	+1.2V_VPCIE
AD24	PCIE_CALRP	R172	EV@562/F_4	
AB24	PCIE_CALI	R167	EV@1.47K/F_4	

B1B:PCIE_CALRN(ball AE24) need change to +1.2V_VPCIE

FOR M52P,M54P,M56P
PCIE_CALRN = 2K
PCIE CALRP = 562R
PCIE CALI = 1.47K

EV@M56-P B13



E3A:Add U65 for M56 PLTRST#

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Quanta Computer Inc.

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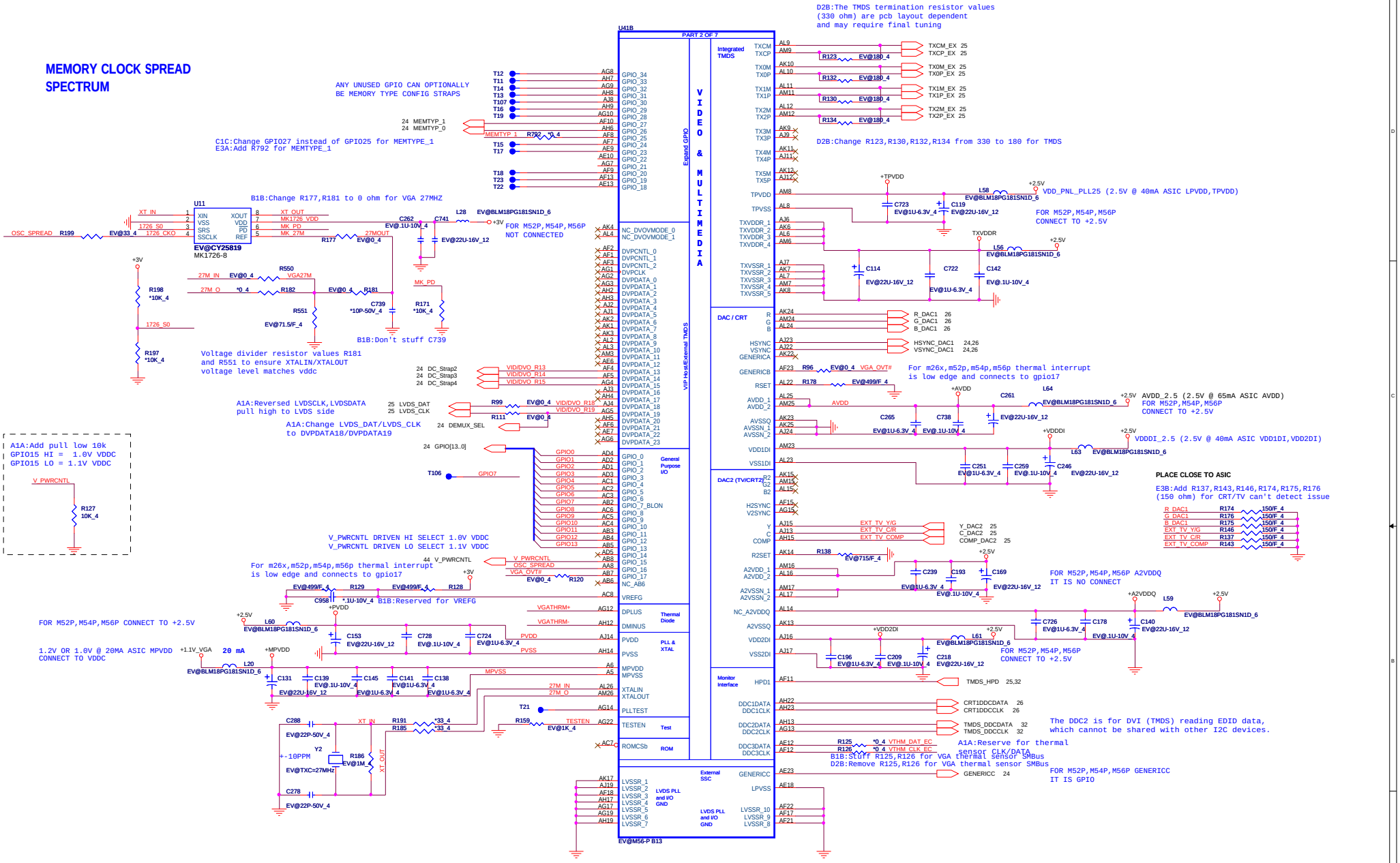
MEMORY CLOCK SPREAD SPECTRUM



If memory interface has to be up to 600Mhz or above, the GPU core voltage and memory I/O voltage may need to be increased to 1.2~1.3V and 2.0V

A1A:Change to VGA_MEM_IO

U41E

PART 5 OF 7

POWER

Memory I/O

I/O

Core

I/O Internal

LVDS PLL, I/O

Memory I/O Clock

PCI-Express

EV@M56-P B13

1.2V ASIC PCIE_PVDD_12 @ 100mA, PCIE_VDDR_12 @ 2000mA

FOR M52P,M54P,M56P CONNECT TO +1.2V

1.2V OR 1.0V @ 18A ASIC VDDC,VDDCI

D2B:Add R778,Q56,Q57 for VGA +3V power sequence

VDD_PNL_PLL25 (2.5V @ 40mA ASIC LPVDD,TPVDD)

A1A:Change to VGA_MEM_IO

GENERICD : FOR M56P IT IS A BACK BIAS REGULATOR CONTROL

U41G

PART 7 OF 7

Forward Compatibility

Control and External SSC

LVDS channel

EV@M56-P B13

Panel power(LCDVCC) control

GENERICD->FOR M56P IT IS A BACK BIAS REGULATOR CONTROL

E3A:Add R789 for G966_VIN,change source to +1.8VSUS

D2B:Add R778,R780 for +1.2V_VPCIE

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Quanta Computer Inc.

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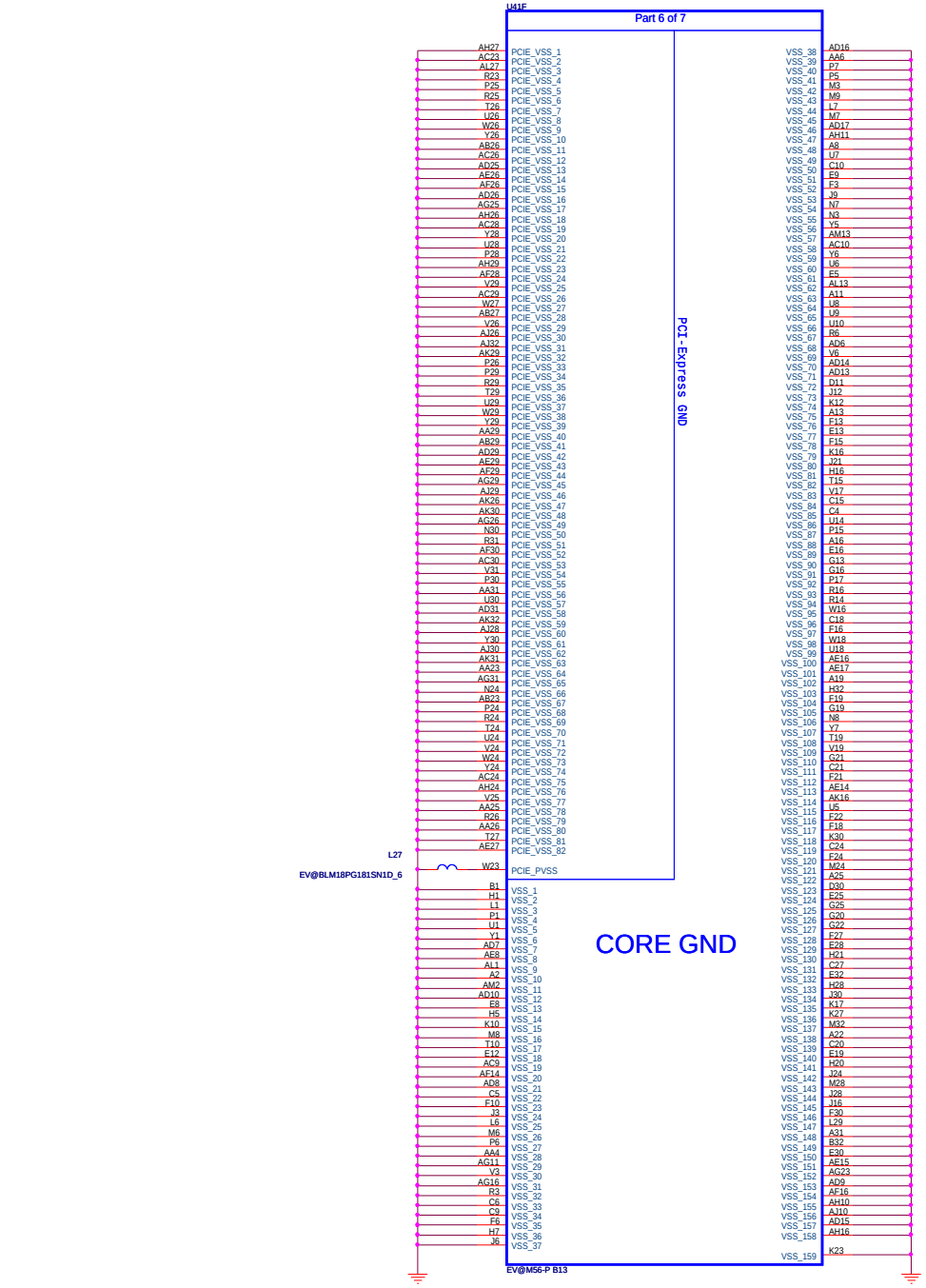

AH27	PCIE_VSS_1
AC23	PCIE_VSS_2
AL27	PCIE_VSS_3
R22	PCIE_VSS_4
P25	PCIE_VSS_5
R25	PCIE_VSS_6
T26	PCIE_VSS_7
U26	PCIE_VSS_8
W26	PCIE_VSS_9
Y26	PCIE_VSS_10
AB26	PCIE_VSS_11
AC26	PCIE_VSS_12
AD25	PCIE_VSS_13
AE26	PCIE_VSS_14
AF26	PCIE_VSS_15
AD26	PCIE_VSS_16
AG25	PCIE_VSS_17
AH26	PCIE_VSS_18
AC28	PCIE_VSS_19
Y28	PCIE_VSS_20
U28	PCIE_VSS_21
P28	PCIE_VSS_22
AH29	PCIE_VSS_23
AF28	PCIE_VSS_24
V29	PCIE_VSS_25
AC29	PCIE_VSS_26
W27	PCIE_VSS_27
AB27	PCIE_VSS_28
V26	PCIE_VSS_29
AJ26	PCIE_VSS_30
AJ32	PCIE_VSS_31
AK29	PCIE_VSS_32
P26	PCIE_VSS_33
P29	PCIE_VSS_34
R29	PCIE_VSS_35
T29	PCIE_VSS_36
U29	PCIE_VSS_37
W29	PCIE_VSS_38
Y29	PCIE_VSS_39
AA29	PCIE_VSS_40
AB29	PCIE_VSS_41
AD29	PCIE_VSS_42
AE29	PCIE_VSS_43
AF29	PCIE_VSS_44
AG29	PCIE_VSS_45
AJ29	PCIE_VSS_46
AK26	PCIE_VSS_47
AK30	PCIE_VSS_48
AG26	PCIE_VSS_49
N30	PCIE_VSS_50
R31	PCIE_VSS_51
AF30	PCIE_VSS_52
AC30	PCIE_VSS_53
V31	PCIE_VSS_54
P30	PCIE_VSS_55
AA31	PCIE_VSS_56
U30	PCIE_VSS_57
AD31	PCIE_VSS_58
AK32	PCIE_VSS_59
AJ28	PCIE_VSS_60
Y30	PCIE_VSS_61
AJ30	PCIE_VSS_62
AK31	PCIE_VSS_63
AA23	PCIE_VSS_64
AG31	PCIE_VSS_65
N24	PCIE_VSS_66
AB23	PCIE_VSS_67
P24	PCIE_VSS_68
R24	PCIE_VSS_69
T24	PCIE_VSS_70
U24	PCIE_VSS_71
V24	PCIE_VSS_72
W24	PCIE_VSS_73
Y24	PCIE_VSS_74
AC24	PCIE_VSS_75
AH24	PCIE_VSS_76
V25	PCIE_VSS_77
AA25	PCIE_VSS_78
R26	PCIE_VSS_79
AA26	PCIE_VSS_80
T27	PCIE_VSS_81
AE27	PCIE_VSS_82
W23	PCIE_PVSS
B1	VSS_1
H1	VSS_2
L1	VSS_3
P1	VSS_4
U1	VSS_5
Y1	VSS_6
AD7	VSS_7
AE8	VSS_8
AL1	VSS_9
A2	VSS_10
AM2	VSS_11
AD10	VSS_12
E8	VSS_13
H5	VSS_14
K10	VSS_15
M8	VSS_16
T10	VSS_17
E12	VSS_18
AC9	VSS_19
AF14	VSS_20
AD8	VSS_21
C5	VSS_22
F10	VSS_23
J3	VSS_24
L6	VSS_25
M6	VSS_26
P6	VSS_27
AA4	VSS_28
AG11	VSS_29
V3	VSS_30
AG16	VSS_31
R3	VSS_32
C6	VSS_33
C9	VSS_34
F6	VSS_35
H7	VSS_36
J6	VSS_37

VSS_38	AD16
VSS_39	AA6
VSS_40	P7
VSS_41	P5
VSS_42	M3
VSS_43	M9
VSS_44	L7
VSS_45	M7
VSS_46	AD17
VSS_47	AH11
VSS_48	A8
VSS_49	U7
VSS_50	C10
VSS_51	E9
VSS_52	F3
VSS_53	J9
VSS_54	N7
VSS_55	N3
VSS_56	Y5
VSS_57	AM13
VSS_58	AC10
VSS_59	Y6
VSS_60	U6
VSS_61	E5
VSS_62	AL13
VSS_63	A11
VSS_64	U8
VSS_65	U9
VSS_66	U10
VSS_67	R6
VSS_68	AD6
VSS_69	V6
VSS_70	AD14
VSS_71	AD13
VSS_72	D11
VSS_73	J12
VSS_74	K12
VSS_75	A13
VSS_76	F13
VSS_77	E13
VSS_78	F15
VSS_79	K16
VSS_80	J21
VSS_81	H16
VSS_82	T15
VSS_83	V17
VSS_84	C15
VSS_85	C4
VSS_86	U14
VSS_87	P15
VSS_88	A16
VSS_89	E16
VSS_90	G13
VSS_91	G16
VSS_92	P17
VSS_93	R16
VSS_94	R14
VSS_95	W16
VSS_96	C18
VSS_97	F16
VSS_98	W18
VSS_99	U18
VSS_100	AE16
VSS_101	AE17
VSS_102	A19
VSS_103	H32
VSS_104	F19
VSS_105	G19
VSS_106	N8
VSS_107	Y7
VSS_108	T19
VSS_109	V19
VSS_110	G21
VSS_111	C21
VSS_112	F21
VSS_113	AE14
VSS_114	AK16
VSS_115	U5
VSS_116	F22
VSS_117	F18
VSS_118	K30
VSS_119	C24
VSS_120	F24
VSS_121	M24
VSS_122	A25
VSS_123	D30
VSS_124	E25
VSS_125	G25
VSS_126	G20
VSS_127	G22
VSS_128	F27
VSS_129	E28
VSS_130	H21
VSS_131	C27
VSS_132	E32
VSS_133	H28
VSS_134	J30
VSS_135	K17
VSS_136	K27
VSS_137	M32
VSS_138	A22
VSS_139	C20
VSS_140	E19
VSS_141	H20
VSS_142	J24
VSS_143	M28
VSS_144	J28
VSS_145	J16
VSS_146	F30
VSS_147	L29
VSS_148	A31
VSS_149	B32
VSS_150	E30
VSS_151	AE15
VSS_152	AG23
VSS_153	AD9
VSS_154	AF16
VSS_155	AH10
VSS_156	AJ10
VSS_157	AD15
VSS_158	AH16
VSS_159	K23

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Quanta Computer Inc.

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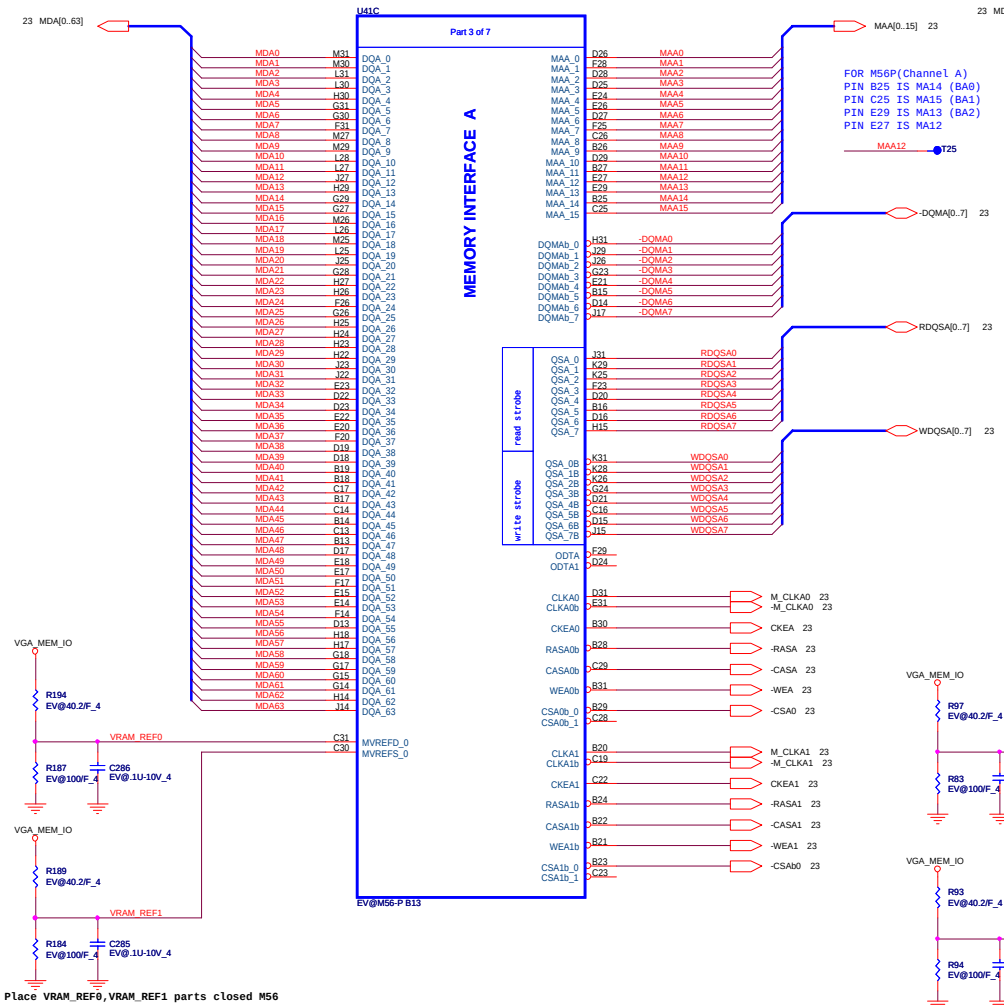
RV410 MEMORY CHANNELS A and B

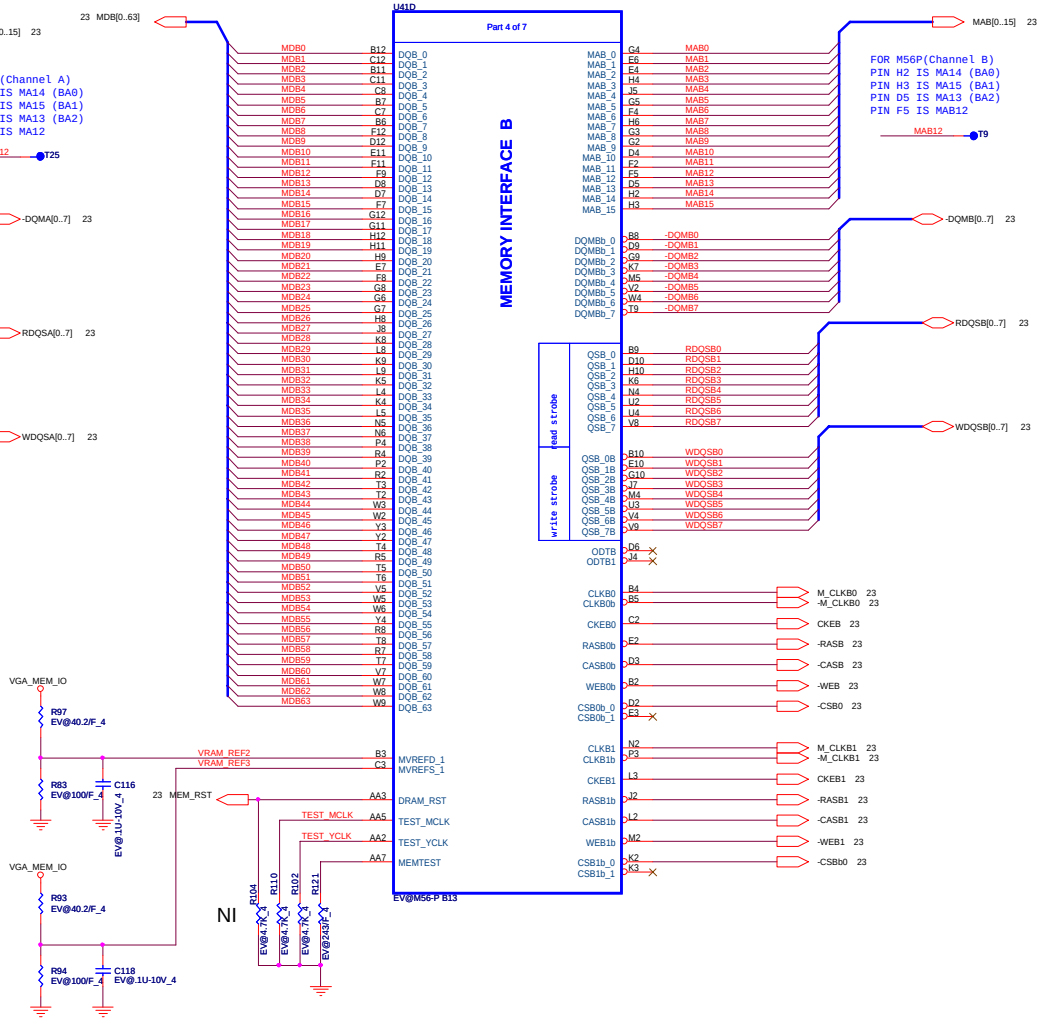
Channel A



Place VRAM_REF0,VRAM_REF1 parts closed M56

Reference voltage per channel (memory data/strobe)
MVREFD_[0:1] (0.7 * VDDR1) (for GDDR3)
MVREFS_[0:1] (0.7 * VDDR1) (for GDDR3)

Channel B



Reference voltage per channel (memory data/strobe)
MVREFD_[0:1] (0.7 * VDDR1) (for GDDR3)
MVREFS_[0:1] (0.7 * VDDR1) (for GDDR3)

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Quanta Computer Inc.

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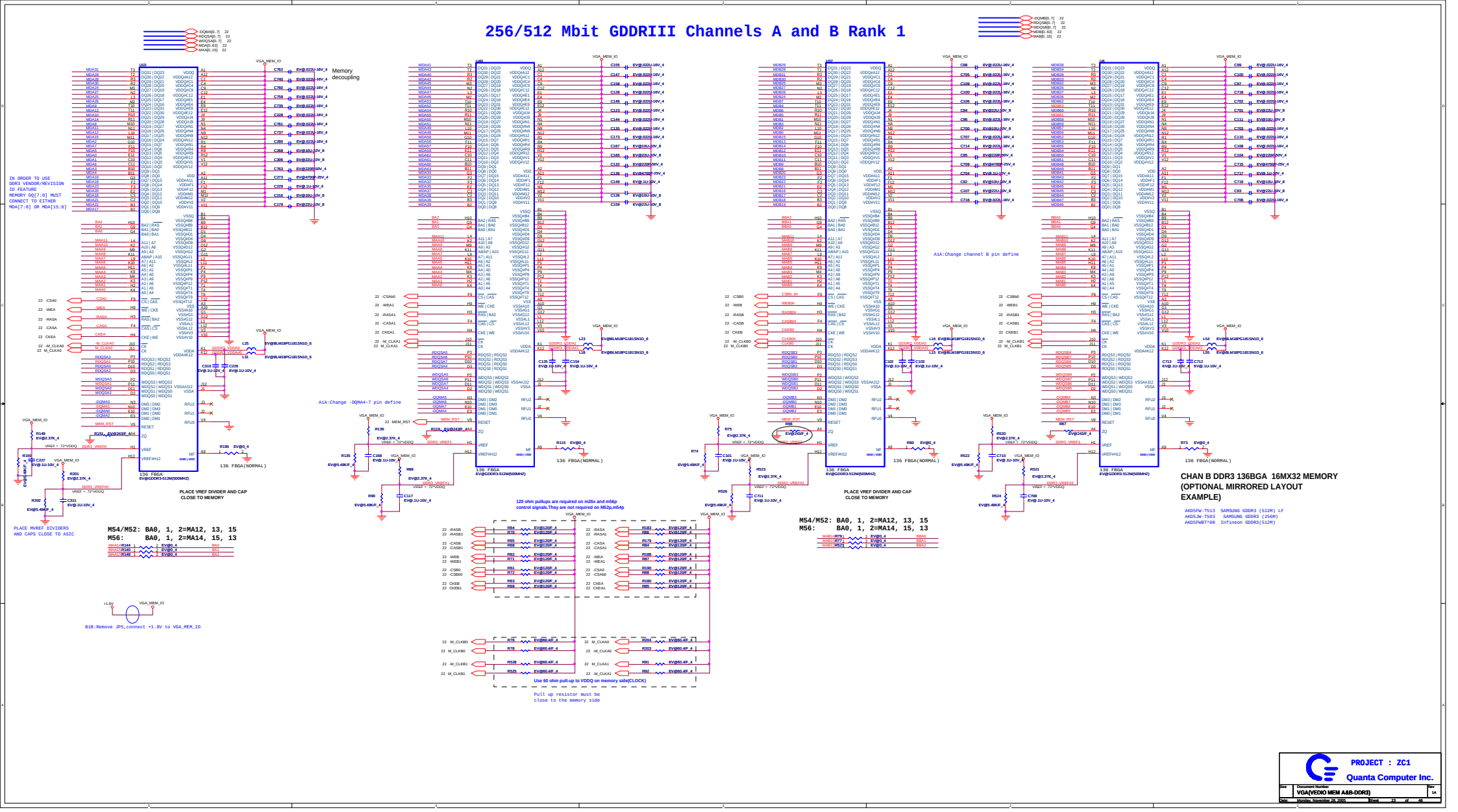
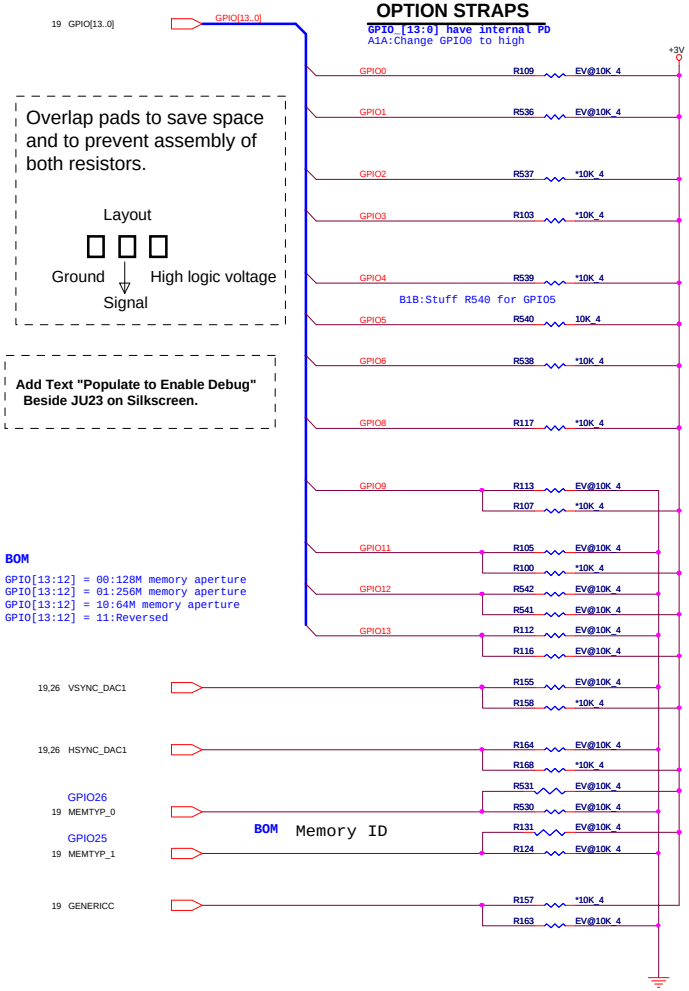
256/512 Mbit GDDRIII Channels A and B Rank 1



OPTION STRAPS

GPIO_[13:0] have internal Pd
A1A:Change GPIO0 to high



Overlap pads to save space and to prevent assembly of both resistors.

Layout

Ground High logic voltage

Signal

Add Text "Populate to Enable Debug" Beside JU23 on Silkscreen.

BOM

GPIO[13:12] = 00:128M memory aperture
GPIO[13:12] = 01:256M memory aperture
GPIO[13:12] = 10:64M memory aperture
GPIO[13:12] = 11:Reversed

BOM Memory ID

M56-P Strap

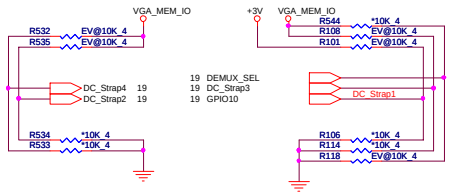
STRAPS	PIN	DESCRIPTION OF RECOMMENDED SETTING	RECOMMENDED
STRAP_B_PTX_PWRS_ENB	GPIO0	TRANSMITTER POWER SAVINGS ENABLE - FULL TX OUTPUT SWING	INSTALL 10K RESISTOR
STRAP_B_PTX_DEEMPH_EN	GPIO1	TRANSMITTER DE-EMPHASIS ENABLE FOR M26X,M56P: INSTALL WITH ATI RS480,RS400,RX480, RC410,RS482 CHIPSETS DO NOT INSTALL WITH INTEL 915PM CHIPSET FOR M5X - INSTALL	TBD
RSVD	GPIO(3:2)	NO ATI FEATURE ENABLED	DO NOT INSTALL 10K RESISTORS
REVERSE LANES DEBUG ACCESS	GPIO4	NO DEBUG ACCESS (M52P,M54P,M56P)	DO NOT INSTALL 10K RESISTOR
STRAP_FORCE_COMPLIANCE RSVD	GPIO5	sets the desired PCIE PLL bandwidth for M5x parts	DO NOT INSTALL 10K RESISTOR
COMMON MODE RANGE	GPIO6	NO ATI FEATURE ENABLED (M52P,M54P,M56P)	DO NOT INSTALL 10K RESISTOR
DEBUG ACCESS FORCE_COMPLIANCE	GPIO8	DON'T FORCE COMPLIANCE STATE(M52P,M54P,M56P)	DO NOT INSTALL 10K RESISTOR
ROMIDCFG(3:0) MEMORY APERTURE SIZE	GPIO(9,13:11)	IF NO ROM GPIO11(M26X) AND GPIO12,13(M52,M54,M56) SET MEMORY APERTURE SIZE 000x - No ROM, MEM_AP_SIZE=00(128MB) 001x - No ROM,MEM_AP_SIZE=01(256MB) 010x - No Rom, MEM_AP_SIZE=10(64MB) 011x - No ROM,MEM_AP_SIZE=11(Reserved) 1000 - Parallel ROM, chip IDis from ROM 1001 - Serial AT25F1024 ROM (Atmel), chip IDis from ROM 1010 - Serial AT45DB011 ROM (Atmel), chip IDis from ROM 1011 - Serial M25P10 ROM (ST), chip IDis from ROM **1100 - Serial M25P05 ROM (ST), chip IDis from ROM** 1100 - Serial NX25F011B ROM (ISSI), chip IDis from ROM	
VIP_DEVICE	VSYNC	Indicates if any slave VIP host devices drove this pin low during reset. 0- Slave VIP host port deviced present. 1-No slave VIP port devices reporting presence during reset	No default
NO STRAP FUNCTION	H2SYNC, V2SYNC,GENERICC	ATI FEATURE NOT ENABLED (M52P,M54P,M56P)	DO NOT INSTALL 10K RESISTOR
	VSYNC	RSVD	
	HSYNC	RSVD	
	PCIE_TEST	RSVD	

A1A:change ROMIDCFG(3:0) to 0010

Board Straps REV 0.3

STRAPS	PIN	DESCRIPTION	VALUE
MEMTYPE(1:0)	GPIO25,26	MEMORY TYPE AND SPEED SELECT Memory connected to R420 identification for BIOS 00 - Samsung GDDR 3 memory(256Mb) 136 Ball BGA package 01 - Samsung GDDR 3 memory(512Mb) 136 Ball BGA package 10 - Infineon GDDR 3 memory(256Mb) 136 Ball BGA package 11 - Infineon GDDR 3 memory(512Mb) 136 Ball BGA package	00
DC_Strap1	GPIO(10)	Internal TMDS Enabled 0 - Disabled **1 - Enabled**	1
DC_Strap2	LCDDATA(13)	Video Capture Enabled **0 - Disabled** 1 - Enabled	1
DC_Strap3	LCDDATA(14)	HDTV out detect 0 - Detected **1 - Not detected**	1
DC_Strap4, DEMUX_SEL	LCDDATA(15,19)	Video capture enable 00 - DAC2 Off 01 - DAC2 On as CRT **10 - DAC2 On as TVOUT** 11 - DAC2 On as TVOUT and CRT	10
PAL/NTSC	LCDDATA(18)	TVO Standard Default (Resistor pull-up and switch short to GND) **0 - PAL (on board resistor pull-down and switch closed)** **1 -NTSC (on board resistor pull-up)**	1

MEMORY TYPE AND SPEED SELECT



A1A:change video capture enable setting

PROJECT : ZC1

Quanta Computer Inc.

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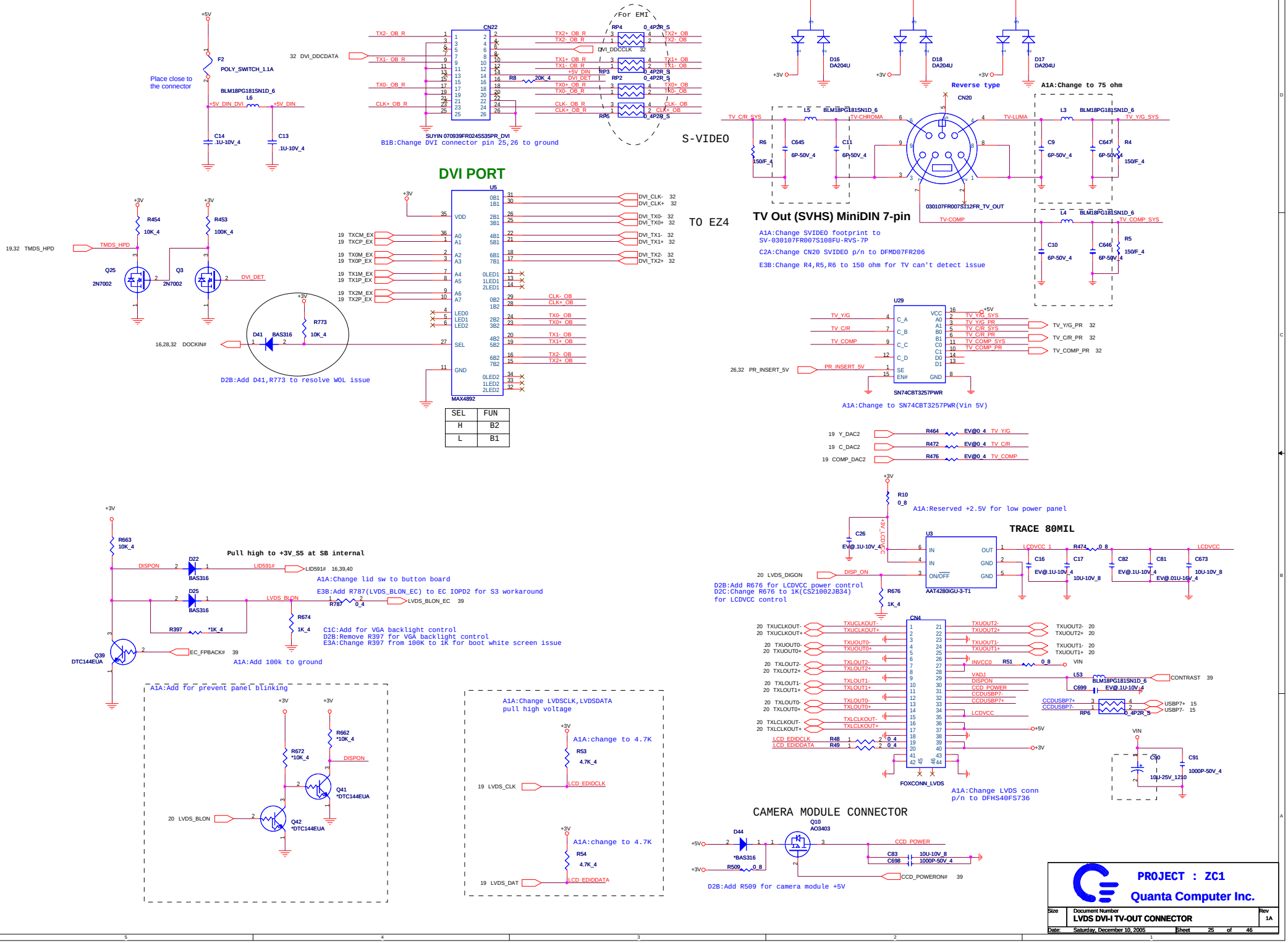
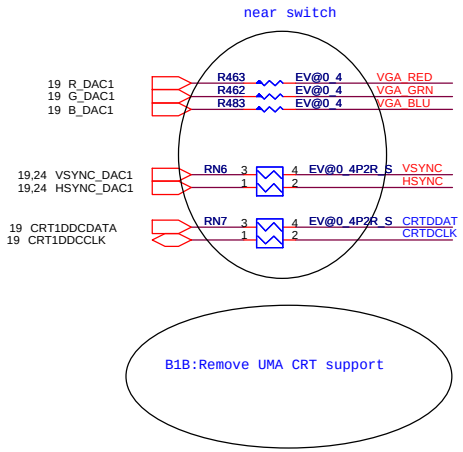
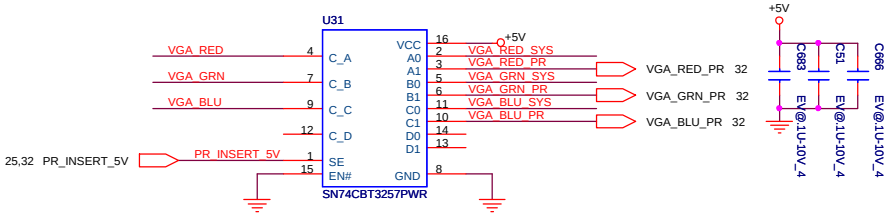
DVI-I CONNECTOR (DVI-D)

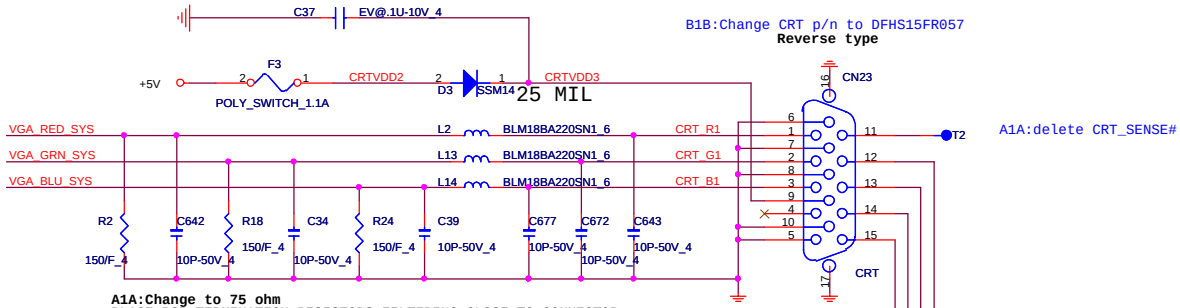






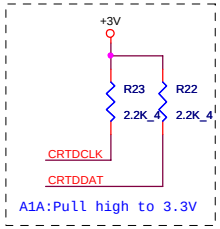
A1A:Change to SN74CBT3257PWR(Vin 5V)

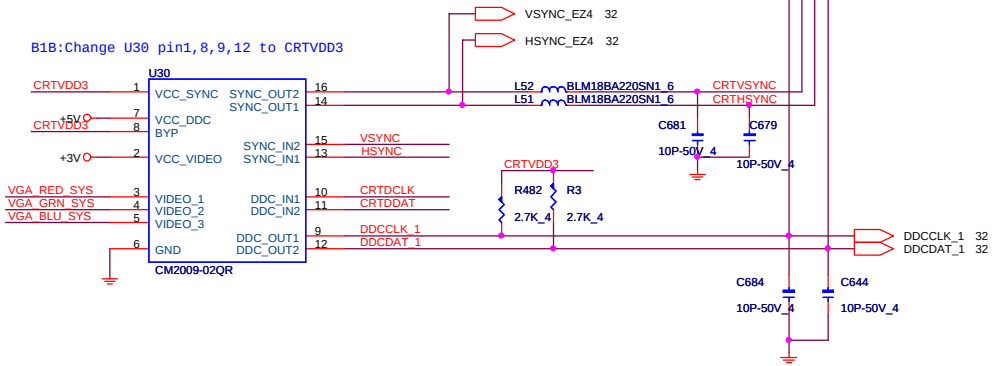
SEL	FUNCTION
LOW	IN_B0
HIGH	IN_B1



A1A:Change to 75 ohm
PLACE RGB TERMINATION RESISTORS,FILTERING CLOSE TO CONNECTOR

E3B:Change R2,R18,R24 to 150 ohm for CRT can't detect issue





PROJECT : ZC1

Quanta Computer Inc.

Size	Document Number	Rev
	CRT-PORT	1A

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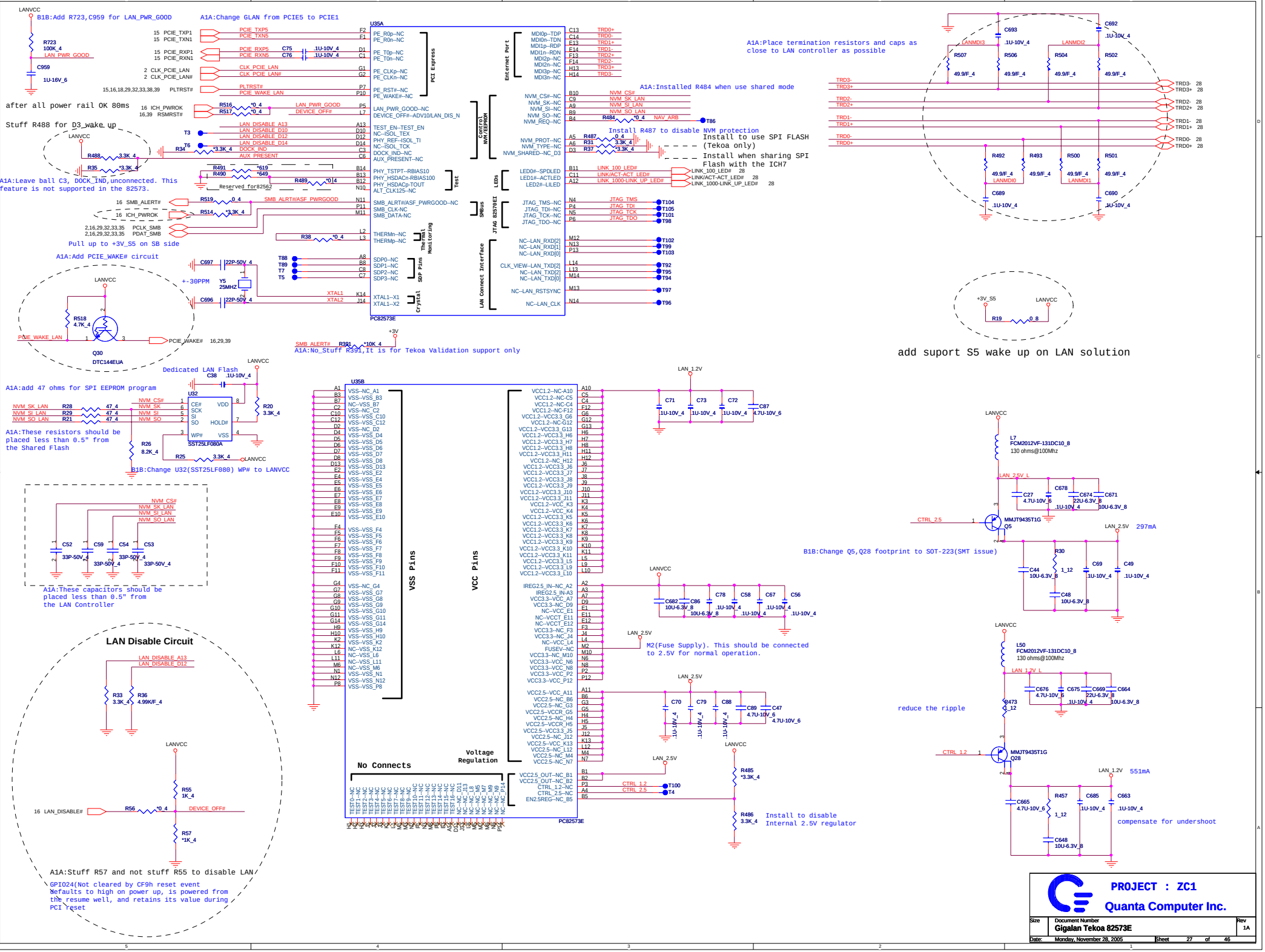
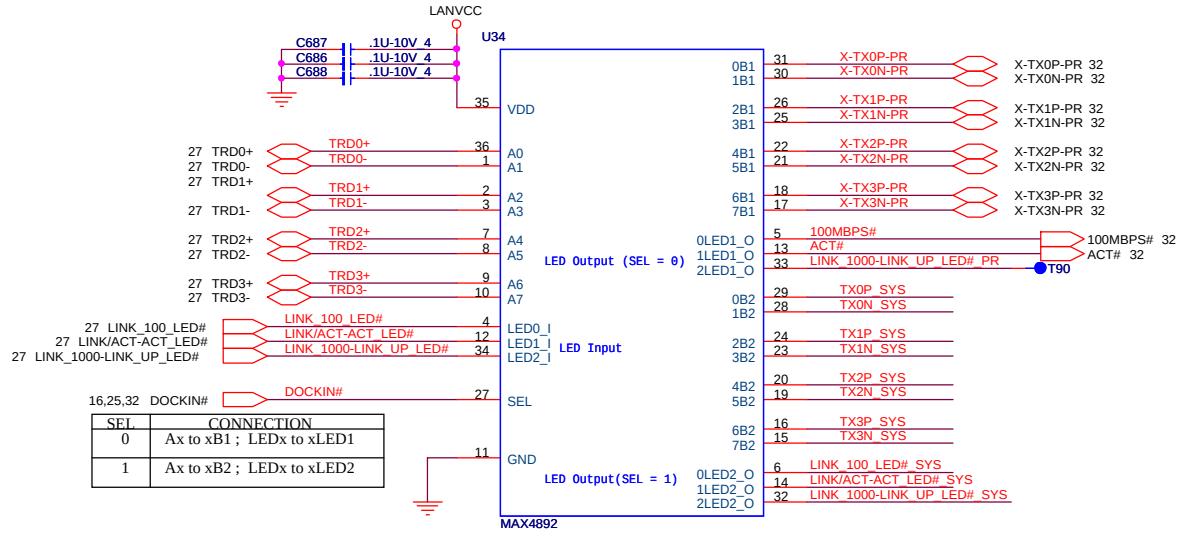

B1B:Add R723,C959 for LAN_PWR_GOOD
A1A:Change GLAN from PCIE5 to PCIE1
U35A
PCI Express
Enternet Port
Control NVM/EEPROM
Test
LEDs
SMBus
JTAG 82576EI
Thermal Monitoring
SDP Pins
Crystal
LAN Connect Interface
PC82573E
after all power rail OK 80ms
Stuff R488 for D3_wake up
A1A:Leave ball C3, DOCK_IND,unconnected. This feature is not supported in the 82573.
Pull up to +3V_S5 on SB side
A1A:Add PCIE_WAKE# circuit
Q30
DTC144EUA
A1A:No_Stuff R391,It is for Tekoa Validation support only
A1A:Installed R484 when use shared mode
Install R487 to disable NVM protection
Install to use SPI FLASH (Tekoa only)
Install when sharing SPI Flash with the ICH7
A1A:Place termination resistors and caps as close to LAN controller as possible
add suport S5 wake up on LAN solution
Dedicated LAN Flash
A1A:add 47 ohms for SPI EEPROM program
A1A:These resistors should be placed less than 0.5" from the Shared Flash
B1B:Change U32(SST25LF080) WP# to LANVCC
A1A:These capacitors should be placed less than 0.5" from the LAN Controller
LAN Disable Circuit
A1A:Stuff R57 and not stuff R55 to disable LAN
GPIO24(Not cleared by CF9h reset event
Defaults to high on power up, is powered from the resume well, and retains its value during PCI reset
U35B
VSS Pins
VCC Pins
Voltage Regulation
No Connects
PC82573E
B1B:Change Q5,Q28 footprint to SOT-223(SMT issue)
M2(Fuse Supply). This should be connected to 2.5V for normal operation.
reduce the ripple
Install to disable Internal 2.5V regulator
compensate for undershoot
PROJECT : ZC1
Quanta Computer Inc.
Gigalan Tekoa 82573E
Monday, November 28, 2005
Sheet 27 of 46

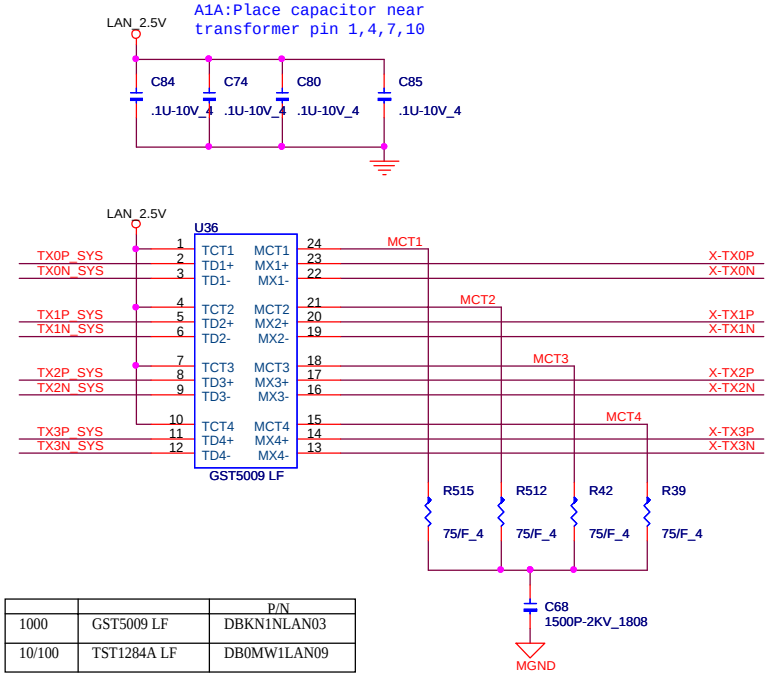


SEL	CONNECTION
0	Ax to xB1 ; LEDx to xLED1
1	Ax to xB2 ; LEDx to xLED2

LED0 Input
0LED1 Output. Connects LED0 to 0LED1 when SEL = 0.
0LED2 Output. Connects LED0 to 0LED2 when SEL = 1.

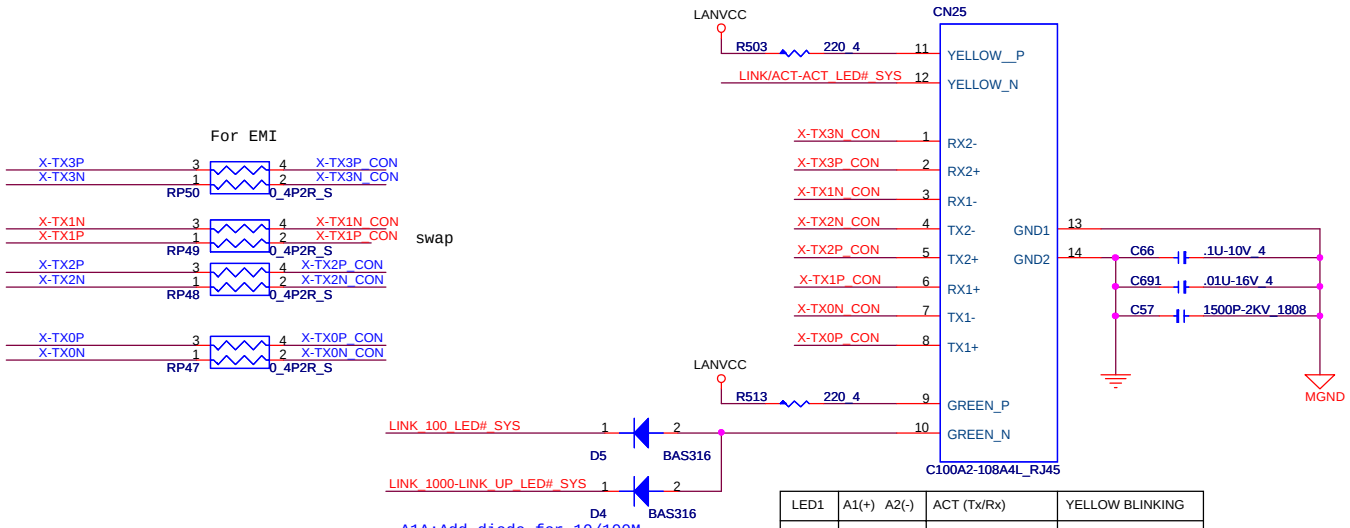
B1B:Change MAX4892 pin define

A1A:Place capacitor near transformer pin 1,4,7,10



		P/N
1000	GST5009 LF	DBKN1NLAN03
10/100	TST1284A LF	DB0MW1LAN09

A1A:Change RJ45 CONN to C100A2-108A4L
A1A:Change RJ45 TX,RX pin define



A1A:Add diode for 10/100M
& 1000M led control

LED1	A1(+) A2(-)	ACT (Tx/Rx)	YELLOW BLINKING
LED2	B1(+) B2(-)	LINK 10/100/1000	GREEN

PROJECT : ZC1

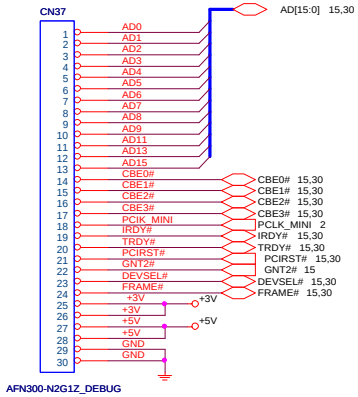
Quanta Computer Inc.

Size	Document Number	Rev
	TRANSFORMER/RJ45	A

Date: Monday, November 28, 2005 Sheet 28 of 46

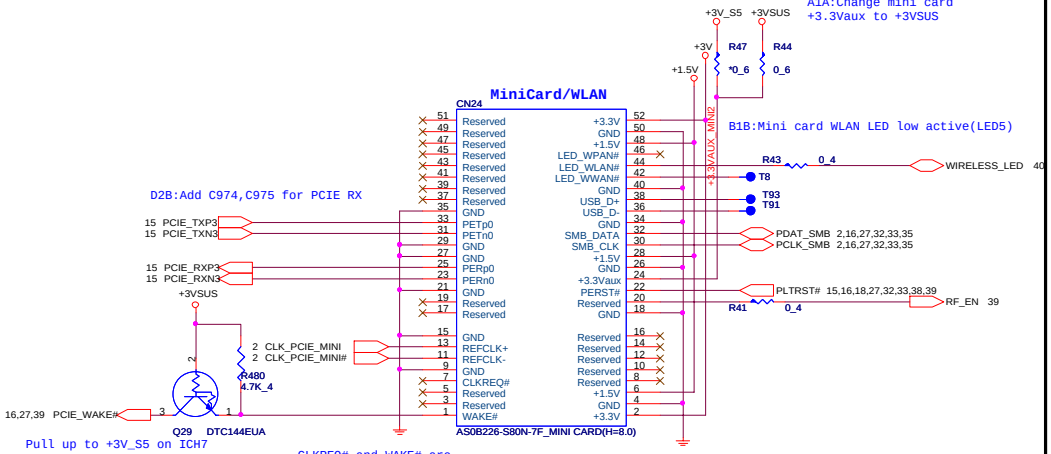
Debug card interface

BOT contact



+3.3V:1000mA
3.3Vaux:330mA
+1.5V:500mA

A1A:Change mini card
+3.3Vaux to +3VSUS

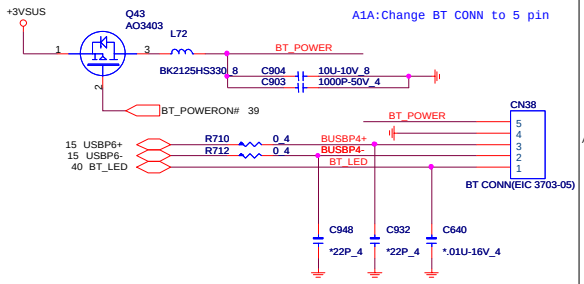


Pull up to +3V_S5 on ICH7

CLKREQ# and WAKE# are
open drain signal

BLUETOOTH MODULE CONNECTOR

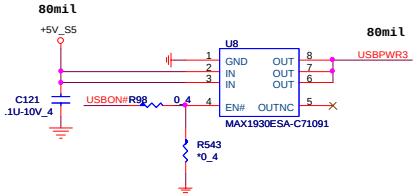
A1A:Change BT CONN to 5 pin



B1B:Change CN38 p/n to DFHD05MS061

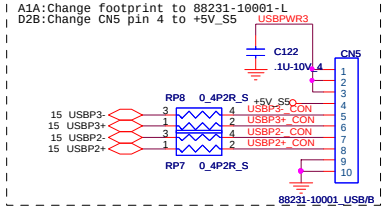
D2B:Change CN38 pin define(1~5) to
meet vertical connector

A1A:In adapter mode, should be powered during S0~S5.
In battery only mode, should be powered during S0 and S3, and not powered during S5

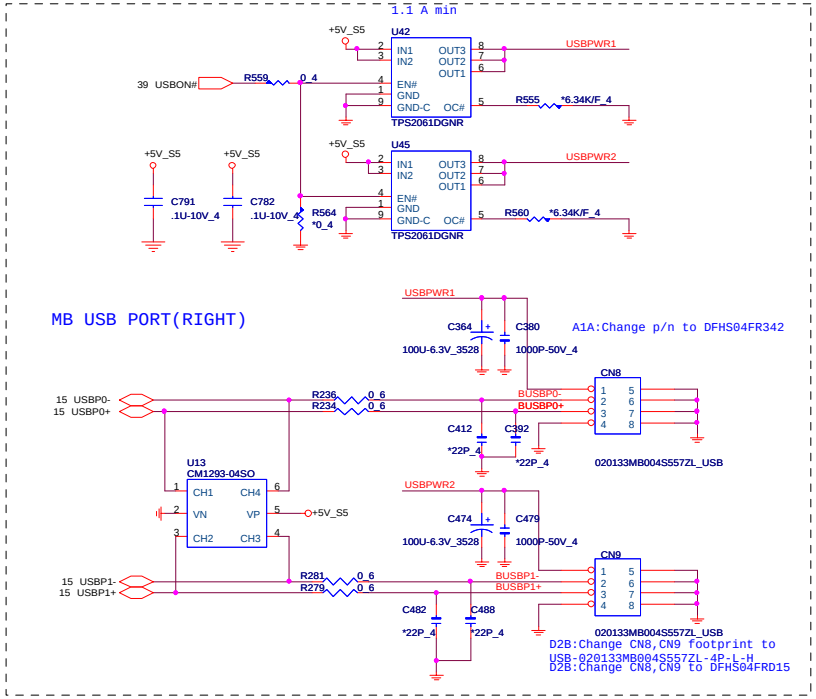


MB USB PORT(REAR)

A1A:Change footprint to 88231-10001-L
D2B:Change CN5 pin 4 to +5V_S5



1.1 A min

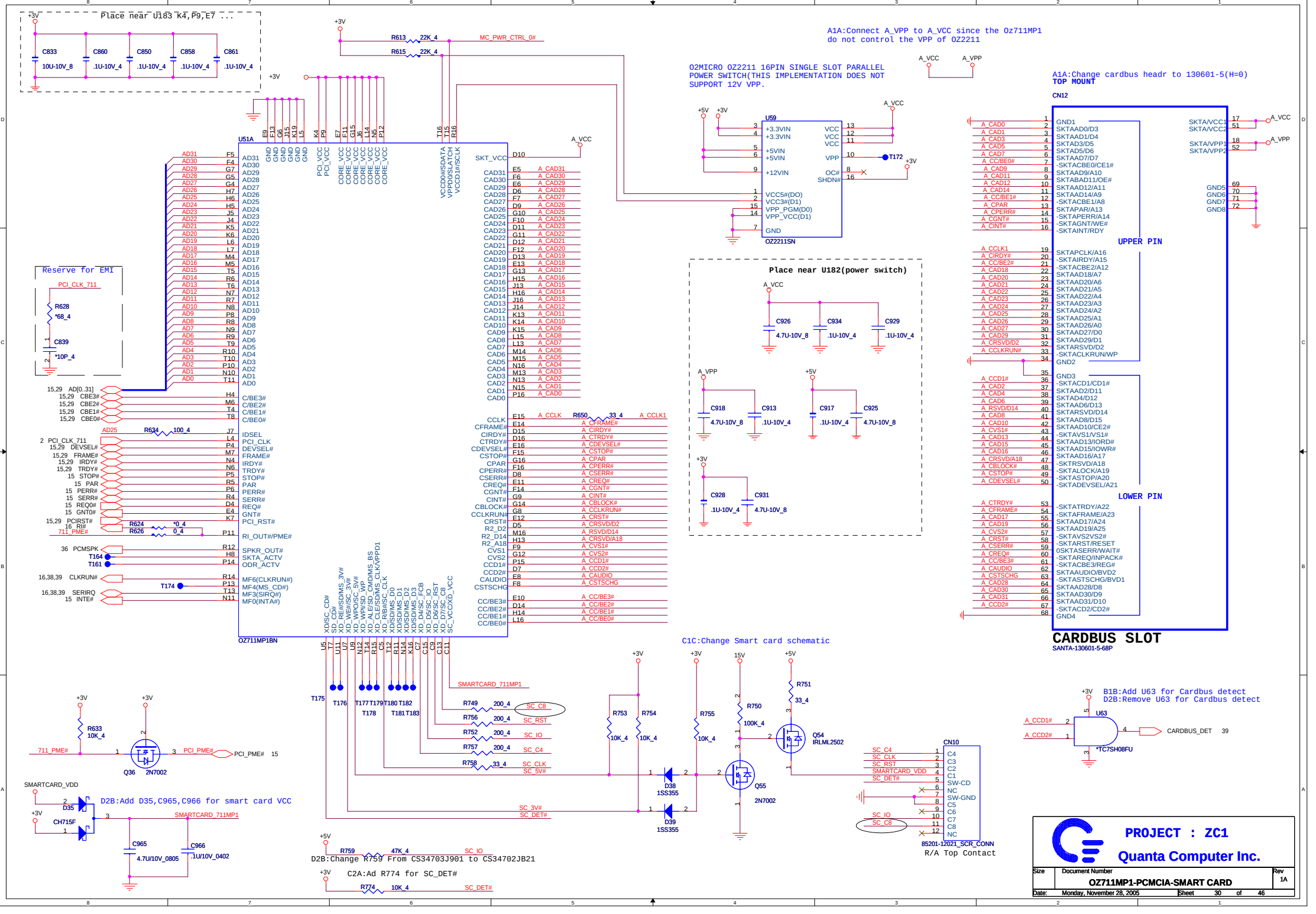


D2B:Change CN8,CN9 footprint to
USB-020133MB004S557ZL-4P-L-H
D2B:Change CN8,CN9 to DFHS04FRD15

PROJECT : ZC1

Quanta Computer Inc.

Size	Document Number	Rev
	DEBUG CARD&PCI-E card&USB	1A
Date: Monday, November 28, 2005	Sheet 29 of 46	


Place near U183 K4,P9,E7 ...
C833 10U-10V_8
C860 .1U-10V_4
C850 .1U-10V_4
C858 .1U-10V_4
C861 .1U-10V_4
R613 22K_4
R615 22K_4
MC_PWR_CTRL_0#
A1A:Connect A_VPP to A_VCC since the Oz711MP1 do not control the VPP of OZ2211
O2MICRO OZ2211 16PIN SINGLE SLOT PARALLEL POWER SWITCH(THIS IMPLEMENTATION DOES NOT SUPPORT 12V VPP.
U59
OZ2211SN
A1A:Change cardbus headr to 130601-5(H=0)
TOP MOUNT
CN12
UPPER PIN
LOWER PIN
CARDBUS SLOT
SANTA-130601-5-68P
U51A
OZ711MP1BN
Reserve for EMI
PCI_CLK_711
R628 *68_4
C839 *10P_4
Place near U182(power switch)
C926 4.7U-10V_8
C934 .1U-10V_4
C929 .1U-10V_4
C918 4.7U-10V_8
C913 .1U-10V_4
C917 .1U-10V_4
C925 4.7U-10V_8
C928 .1U-10V_4
C931 4.7U-10V_8
R634 100_4
R624 *0_4
R626 0_4
711_PME#
PCI_PME#
Q36 2N7002
R633 10K_4
SMARTCARD_VDD
D35 CH715F
D2B:Add D35,C965,C966 for smart card VCC
C965 4.7U/10V_0805
C966 .1U/10V_0402
SMARTCARD_711MP1
C1C:Change Smart card schematic
R749 200_4 SC_C8
R756 200_4 SC_RST
R752 200_4 SC_IO
R757 200_4 SC_C4
R758 33_4 SC_CLK
SC_5V#
SC_3V#
SC_DET#
D38 1SS355
D39 1SS355
Q55 2N7002
Q54 IRLML2502
R750 100K_4
R751 33_4
CN10
85201-12021_SCR_CONN
R/A Top Contact
B1B:Add U63 for Cardbus detect
D2B:Remove U63 for Cardbus detect
U63 *TC7SH08FU
CARDBUS_DET
R759 47K_4
D2B:Change R759 From CS34703J901 to CS34702JB21
C2A:Ad R774 From SC_DET#
R774 10K_4
PROJECT : ZC1
Quanta Computer Inc.
Size
Document Number
OZ711MP1-PCMCIA-SMART CARD
Rev 1A
Date: Monday, November 28, 2005
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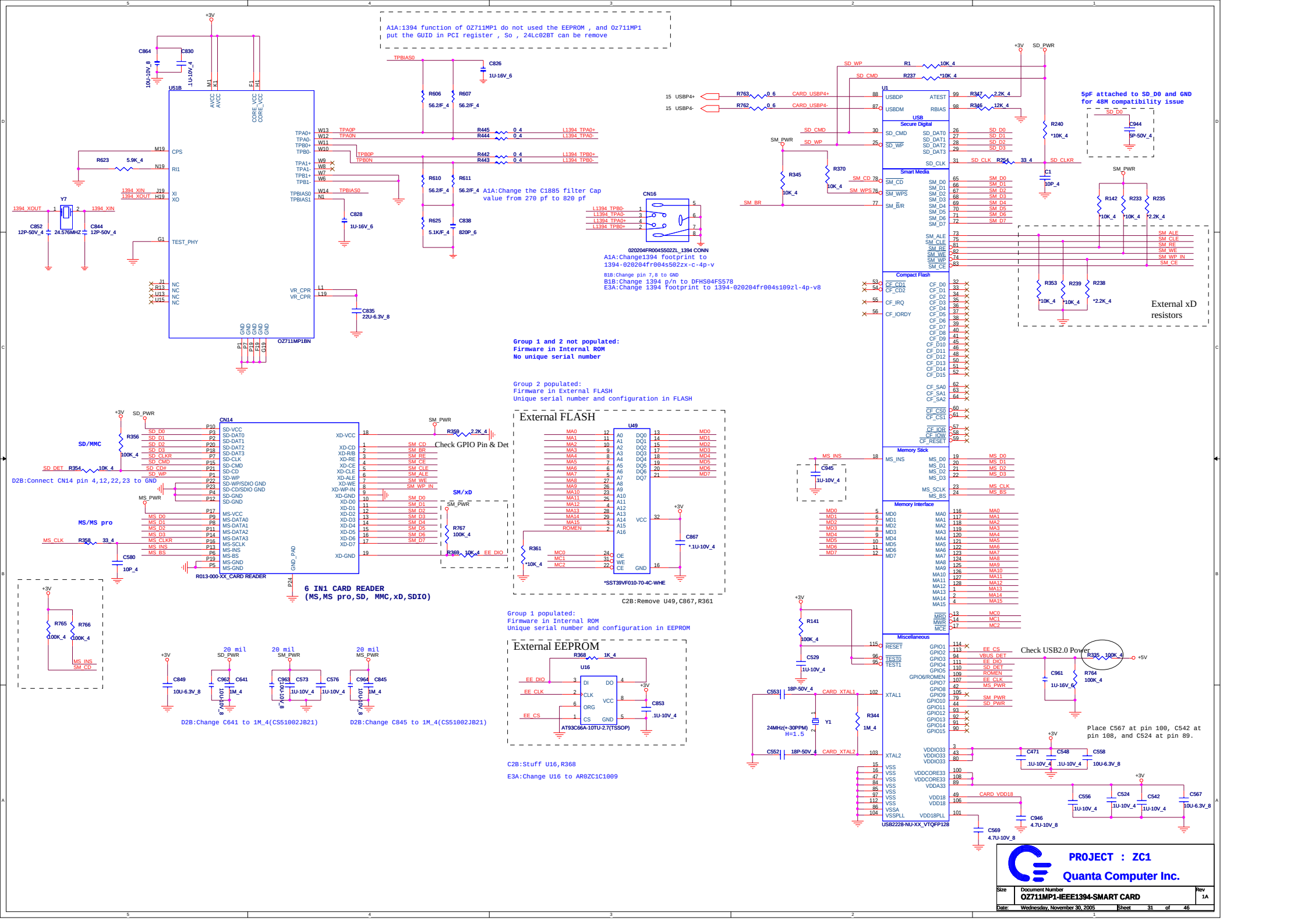
A1A:1394 function of OZ711MP1 do not used the EEPROM , and Oz711MP1 put the GUID in PCI register , So , 24LC02BT can be remove
U51B
OZ711MP1BN
A1A:Change the C1885 filter Cap value from 270 pf to 820 pf
CN16
020204FR004S502ZL_1394 CONN
A1A:Change1394 footprint to 1394-020204fr004s502zx-c-4p-v
B1B:Change pin 7,8 to GND
B1B:Change 1394 p/n to DFHS04FS578
E3A:Change 1394 footprint to 1394-020204fr004s109zl-4p-v8
5pF attached to SD_D0 and GND for 48M compatibility issue
External xD resistors
Group 1 and 2 not populated:
Firmware in Internal ROM
No unique serial number
Group 2 populated:
Firmware in External FLASH
Unique serial number and configuration in FLASH
External FLASH
U49
*SST39VF010-70-4C-WHE
C2B:Remove U49,C867,R361
Group 1 populated:
Firmware in Internal ROM
Unique serial number and configuration in EEPROM
External EEPROM
U16
AT93C66A-10TU-2.7(TSSOP)
C2B:Stuff U16,R368
E3A:Change U16 to AR0ZC1C1009
SD/MMC
D2B:Connect CN14 pin 4,12,22,23 to GND
Check GPIO Pin & Det
SM/xD
MS/MS pro
R013-000-XX_CARD READER
6 IN1 CARD READER
(MS,MS pro,SD, MMC,xD,SDIO)
20 mil
D2B:Change C641 to 1M_4(CS51002JB21)
D2B:Change C845 to 1M_4(CS51002JB21)
USB2228-NU-XX_VTQFP128
Check USB2.0 Power
Place C567 at pin 100, C542 at pin 108, and C524 at pin 89.
PROJECT : ZC1
Quanta Computer Inc.
Size
Document Number
OZ711MP1-IEEE1394-SMART CARD
Rev
1A
Date: Wednesday, November 30, 2005
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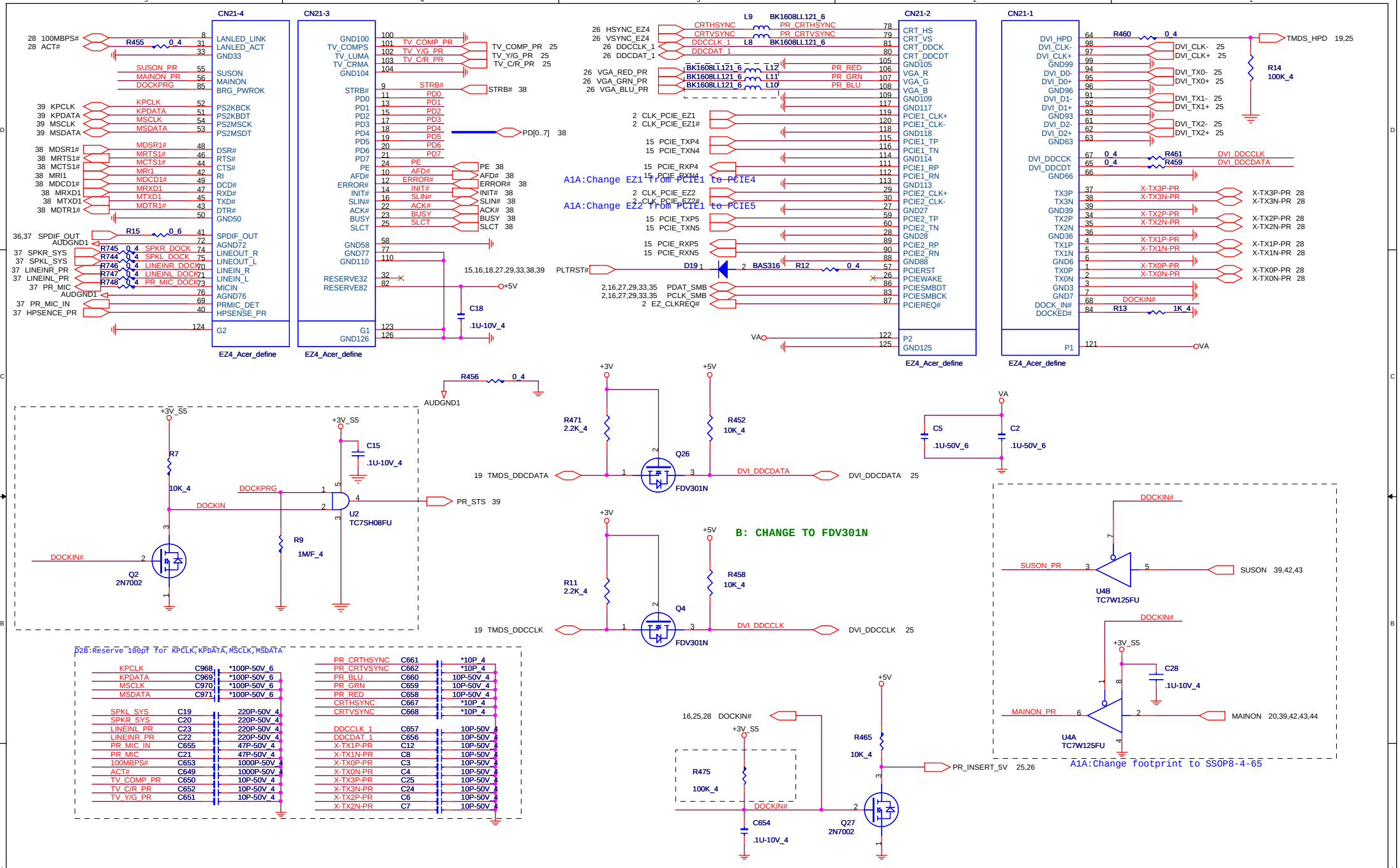
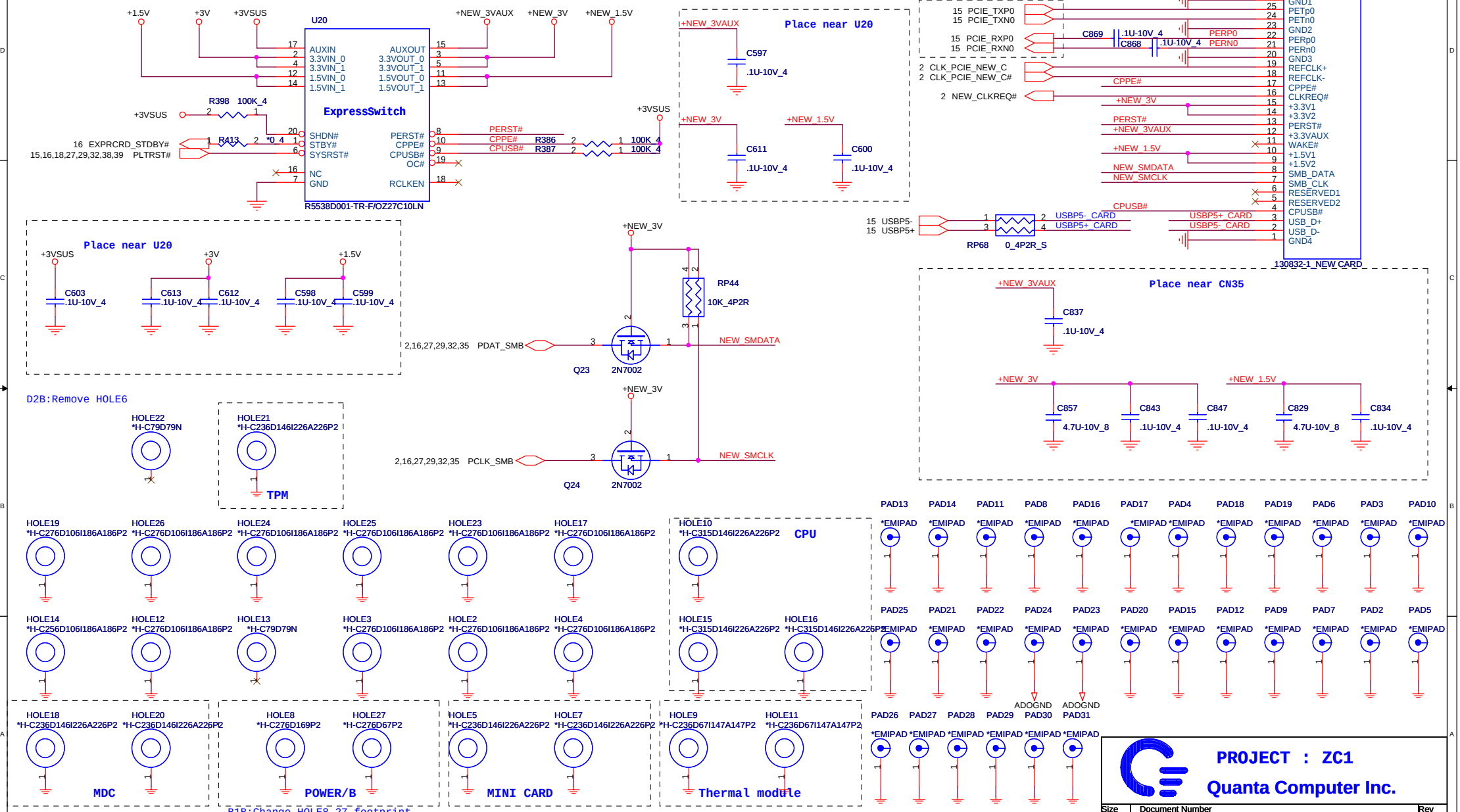

CN21-4
CN21-3
CN21-2
CN21-1
EZ4_Acer_define
A1A:Change EZ1 from PCIE1 to PCIE4
A1A:Change EZ2 from PCIE1 to PCIE5
B: CHANGE TO FDV301N
A1A:Change footprint to SSOP8-4-65
D26:Reserve 100pf for KPCLK,KPDATA,MSCLK,MSDATA
PROJECT : ZC1
Quanta Computer Inc.
Size
Document Number
EZ4 CONN
Rev
1A
Date: Tuesday, December 06, 2005
Sheet 32 of 46

+NEW_1.5V Max. 650mA, Average 500mA.
+NEW_3V Max. 1300mA, Average 1000mA.

A1A:Change New card power sw to Oz27c10

A1A:Change New card to small type(130832-1)



B1B:Change HOLE8,27 footprint

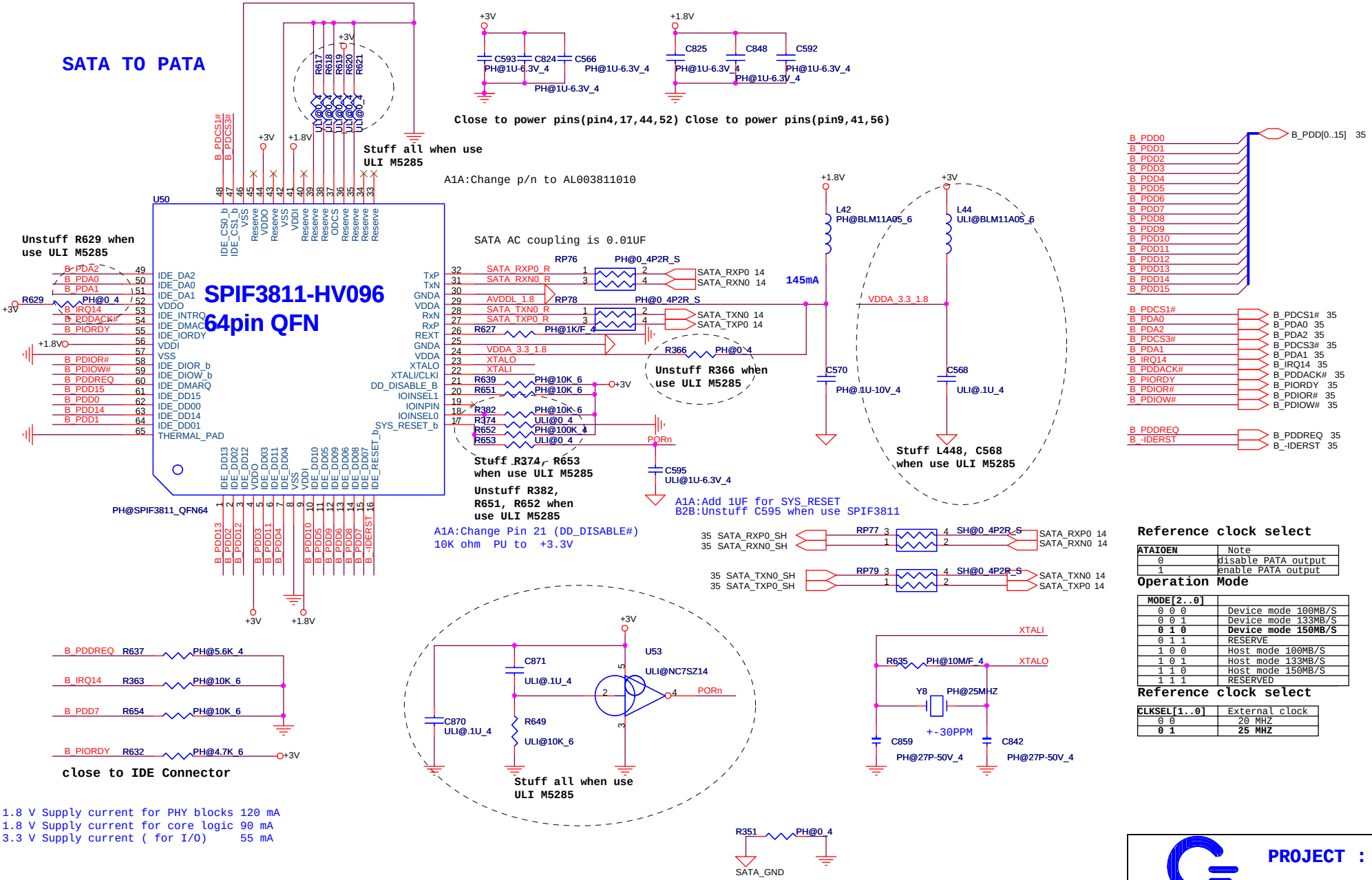
PROJECT : ZC1

Quanta Computer Inc.

Size	Document Number	Rev
	NEW CARD &HOLE	C

Date: Monday, November 28, 2005 Sheet 33 of 46

SATA TO PATA



Reference clock select

ATAIOEN	Note
0	disable PATA output
1	enable PATA output

Operation Mode

MODE[2..0]	
0 0 0	Device mode 100MB/S
0 0 1	Device mode 133MB/S
0 1 0	**Device mode 150MB/S**
0 1 1	RESERVE
1 0 0	Host mode 100MB/S
1 0 1	Host mode 133MB/S
1 1 0	Host mode 150MB/S
1 1 1	RESERVED

Reference clock select

CLKSEL[1..0]	External clock
0 0	20 MHZ
0 1	**25 MHZ**

1.8 V Supply current for PHY blocks 120 mA
1.8 V Supply current for core logic 90 mA
3.3 V Supply current (for I/O) 55 mA

PROJECT : ZC1

Quanta Computer Inc.

Size	Document Number	Rev
	SATA/PATA	A

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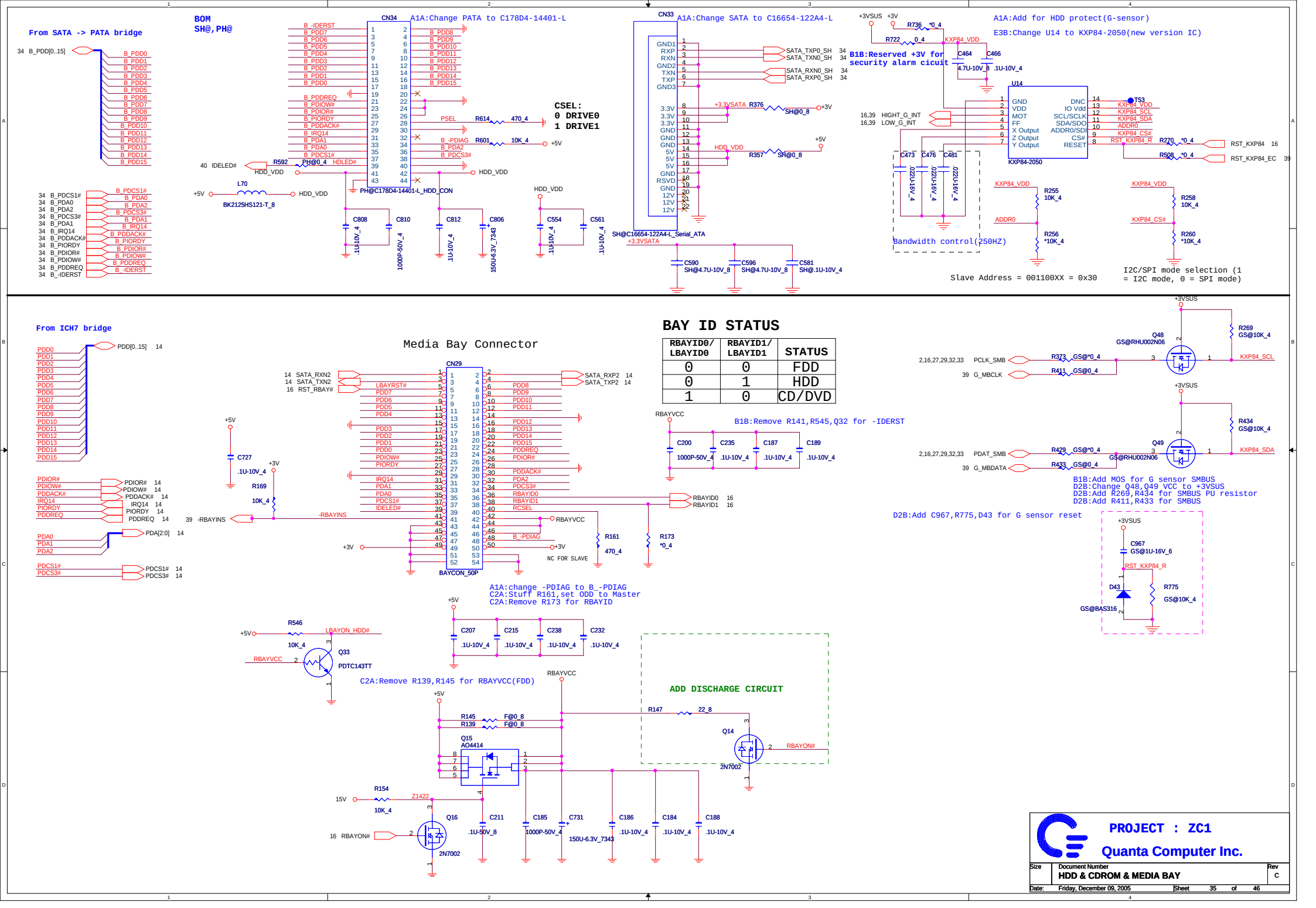
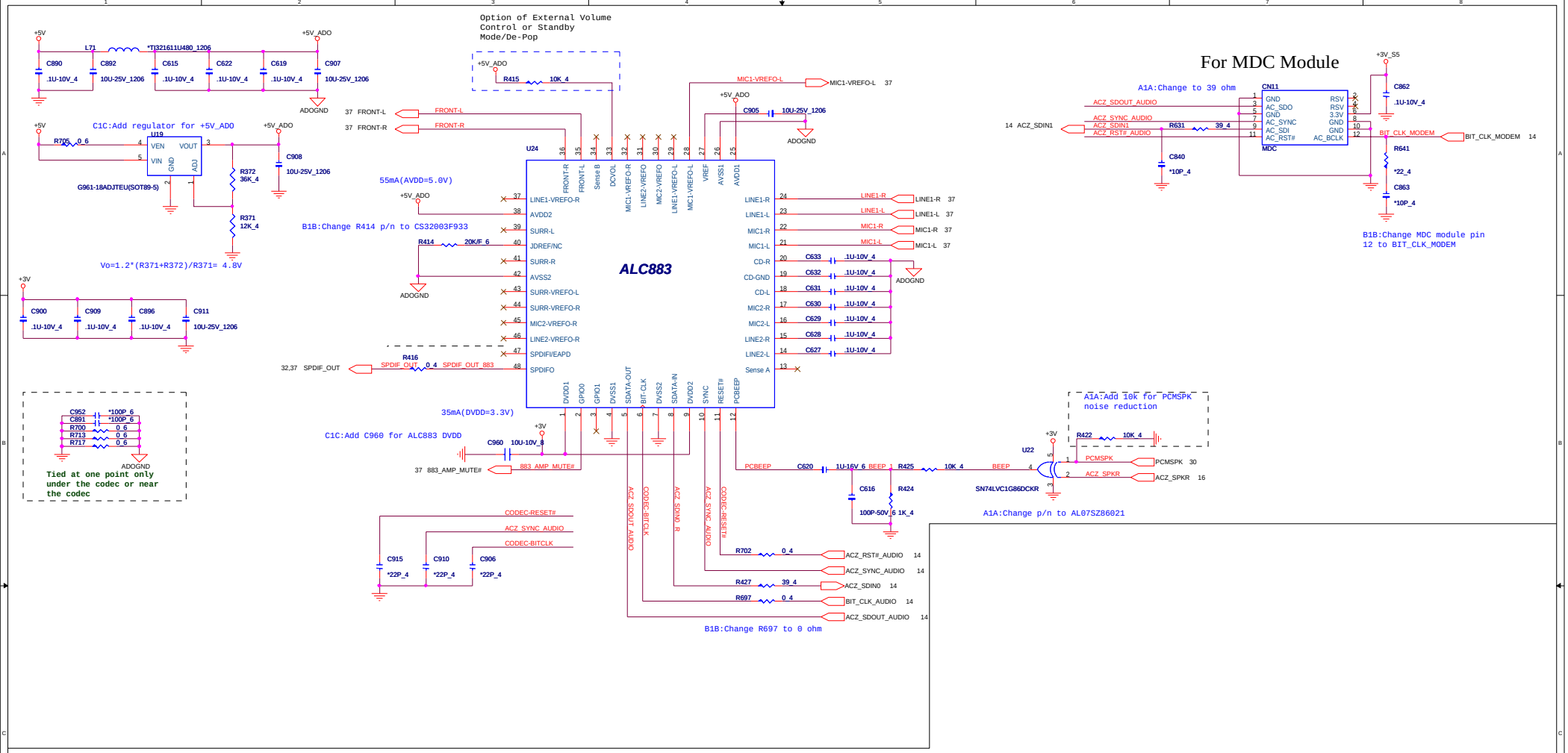


RBAYID0/ LBAYID0	RBAYID1/ LBAYID1	STATUS
0	0	FDD
0	1	HDD
1	0	CD/DVD



PROJECT : ZC1

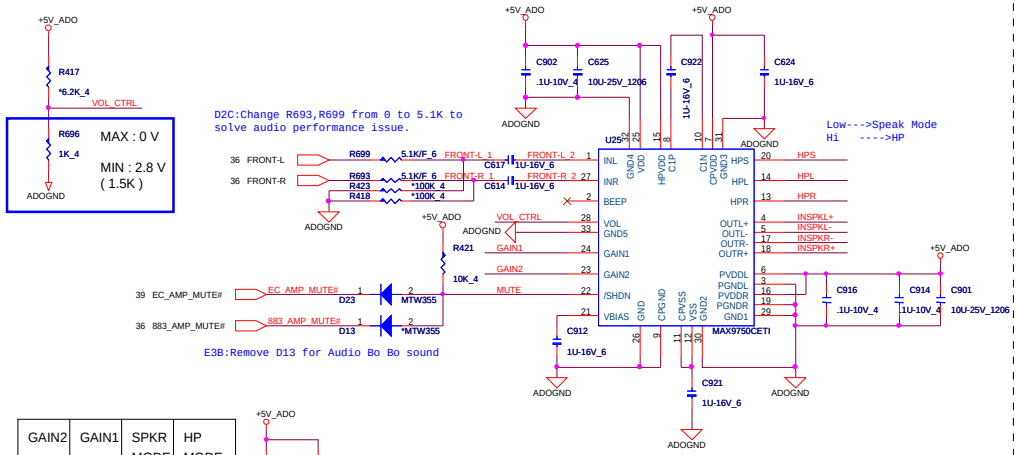
Quanta Computer Inc.

Size	Document Number	Rev
	ALC883 & MDC	1A

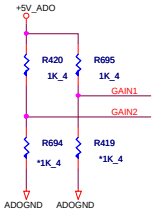
Date: Tuesday, December 06, 2005 Sheet 36 of 46

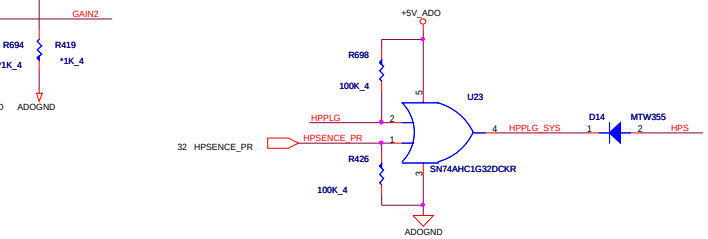
Audio amplifier

A1A:Change audio amplifier to MAX9750
A1A:Change footprint to tqfn28-5x5-5-33p



GAIN2	GAIN1	SPKR MODE	HP MODE
0	0	6	0
0	1	7.5	
1	0	9	3
1	1	10.5	



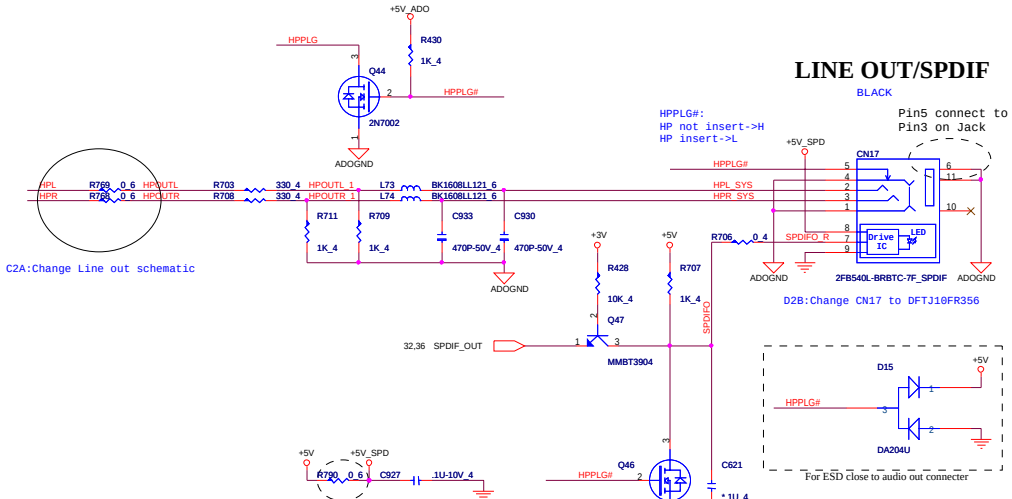


LINE OUT/SPDIF

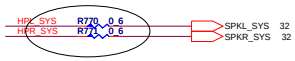
BLACK

HPPLG#:
HP not insert->H
HP insert->L

Pin5 connect to Pin3 on Jack

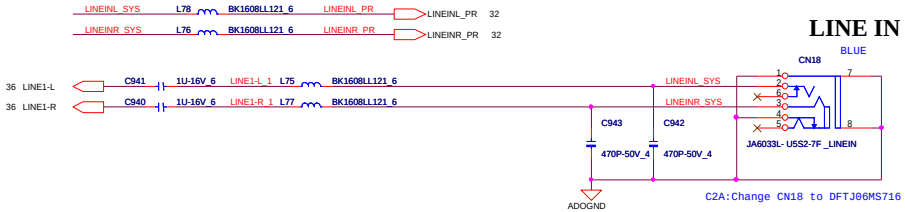


C2A:Change Line out schematic



LINE IN

BLUE

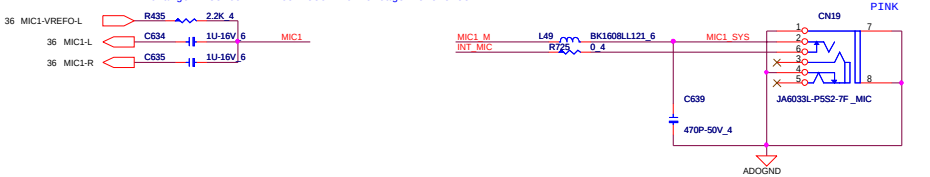


C2A:Change CN18 to DFTJ06MS716

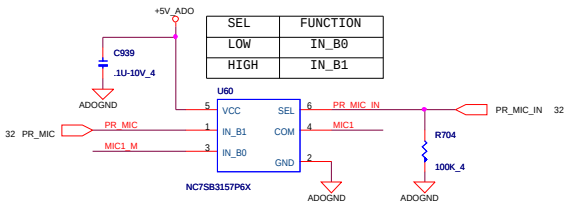
MIC

PINK

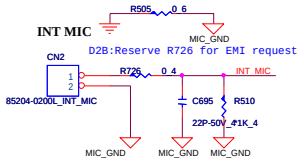
D2B:Change R435 to 2.2K to meet MIC voltage reference



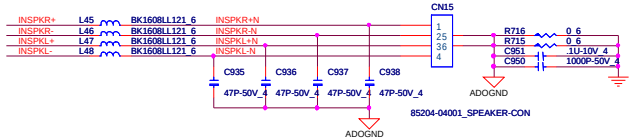
C2A:Change CN19 to DFTJ06MS724



SEL	FUNCTION
LOW	IN_B0
HIGH	IN_B1



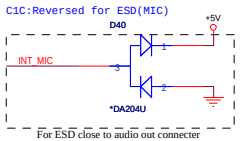
SPEAKER CONNECTOR



A1A:Change Speaker conn footprint

B1B:Change speaker p/n to DFHD04MR701

C1C:Reversed for ESD(MIC)



For ESD close to audio out connecter

PROJECT : ZC1

Quanta Computer Inc.

Size	Document Number	Rev
	AUDIO AMP(MAX9750) / JACK	1A

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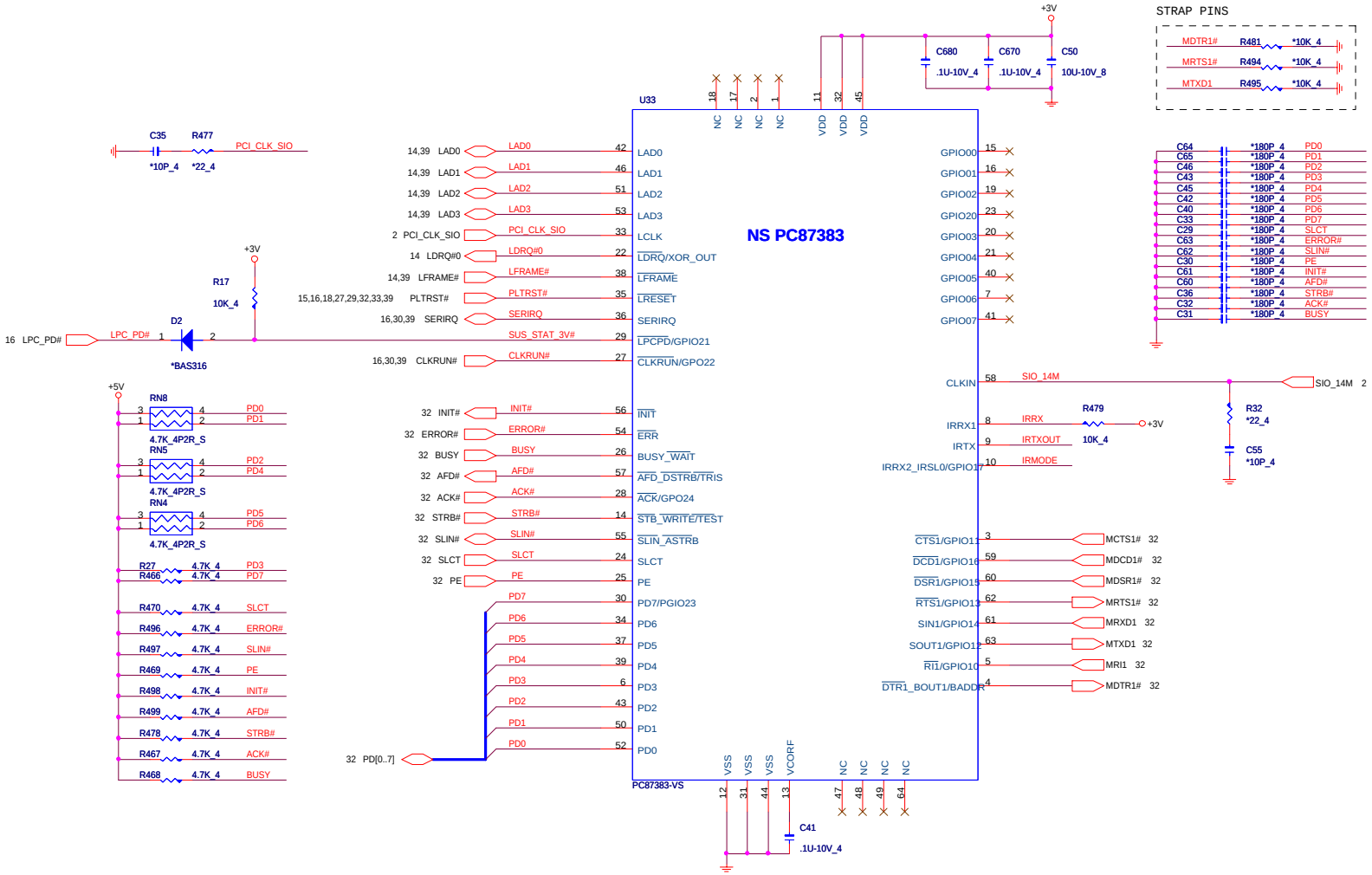
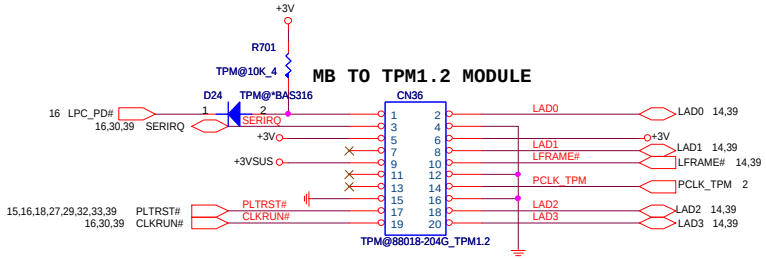
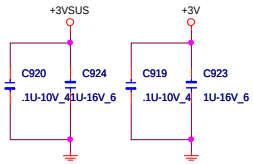


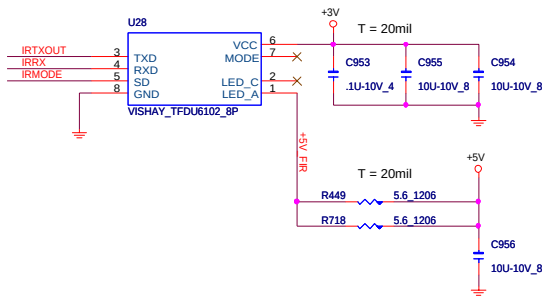


A1A:Change TPM CONN to 88018-204G(Pitch=0.8,H=2.65)

B1B:Change TPM pin define to same as ZH2



FIR



PROJECT : ZC1

Quanta Computer Inc.

Size	Document Number	Rev
	SIO (87383),TPM 1.2	1A

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Adapter ID	
Watt	Voltage
65W	0.66 +/- 0.1V
90W	1.32 +/- 0.1V
135W	1.98 +/- 0.1V
150W	2.64 +/- 0.1V
Un-define	3.3 +/- 0.1V

Should have a 0.1uF capacitor close to every GND-VCC pair + one larger cap on the supply.

I/O Address		
BADDR1-0	Index	Data
0 0	2E	2F
0 1	4E	4F
1 0	(HCFGBAH, HCFGBAL)	(HCFGBAH, HCFGBAL)+1
1 1	Reserved	

LDRQ#(pin 8) internal is no use

A1A:Reserved GSENSOR-X/Y/Z for security alarm cicuit

A1A:Remove REFON pin (DA3 pin 102)

D2B:Add RST_KXP84_EC for G sensor reset(IOPA6)

D2B:Add G-Sensor SMBUS to EC(SCL2,SDA2)

D2B:Change EC_FPBACK# to IOPC6

D2B:Change Cardbus detect to IOPD0

SST 1MB BIOS (AKE35ZAKK17)

ST Micro M29W008AB/AMD-29LV081B/SST39VF080

B1B:Reversed for G sensor buzzer

D2B:Change buzzer power to +5V,increase volume

SHBM=1: Enable shared memory with host BIOS

BIU configuration should match flash speed used

A1A:Reserved for debug use

B1B:Change SW4 p/n to DHP00BB1J03

FOR 97551 ONLY

INTERNAL PULLUP IN SB

PROJECT : ZC1

Quanta Computer Inc.

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	97551 & FLASH	1A

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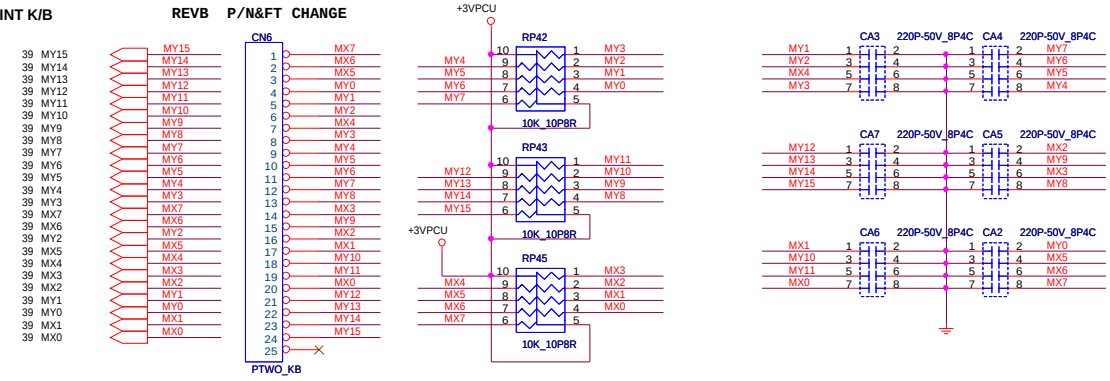
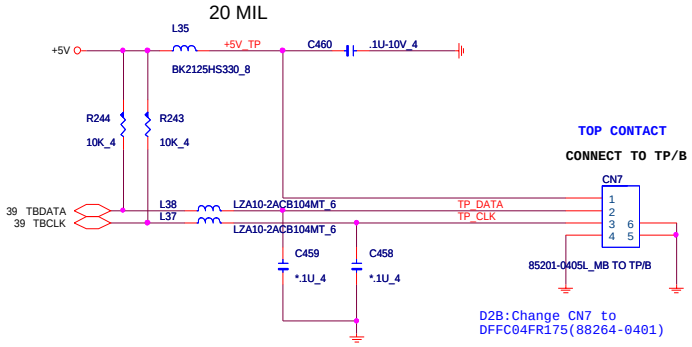
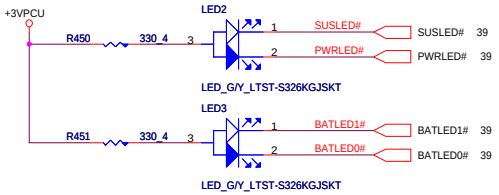
INT K/B

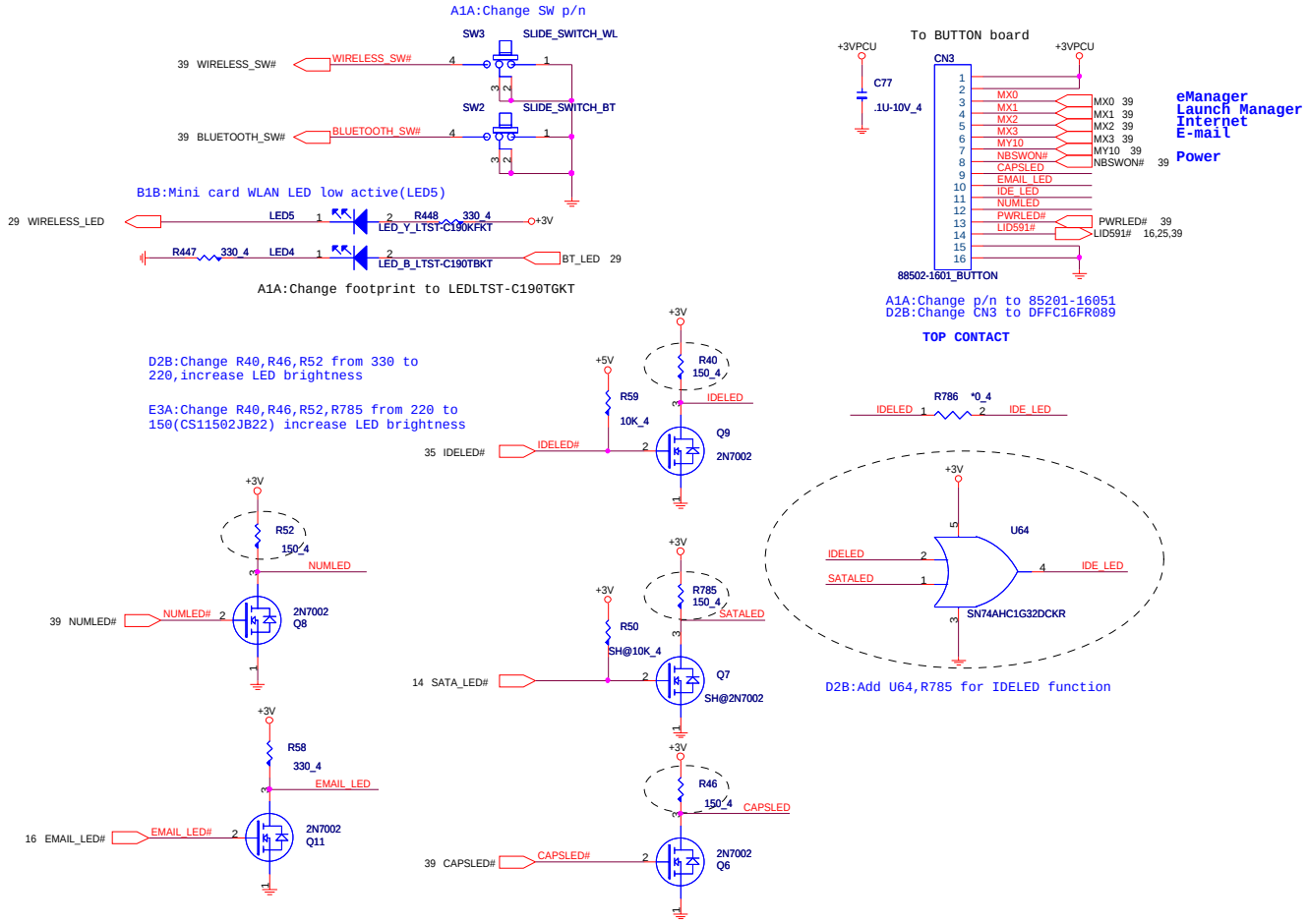
REVB P/N&FT CHANGE



TOUCH PAD







PROJECT : ZC1

Quanta Computer Inc.

Size	Document Number	Rev
	SWITCH,LED,K/B,TP	1A

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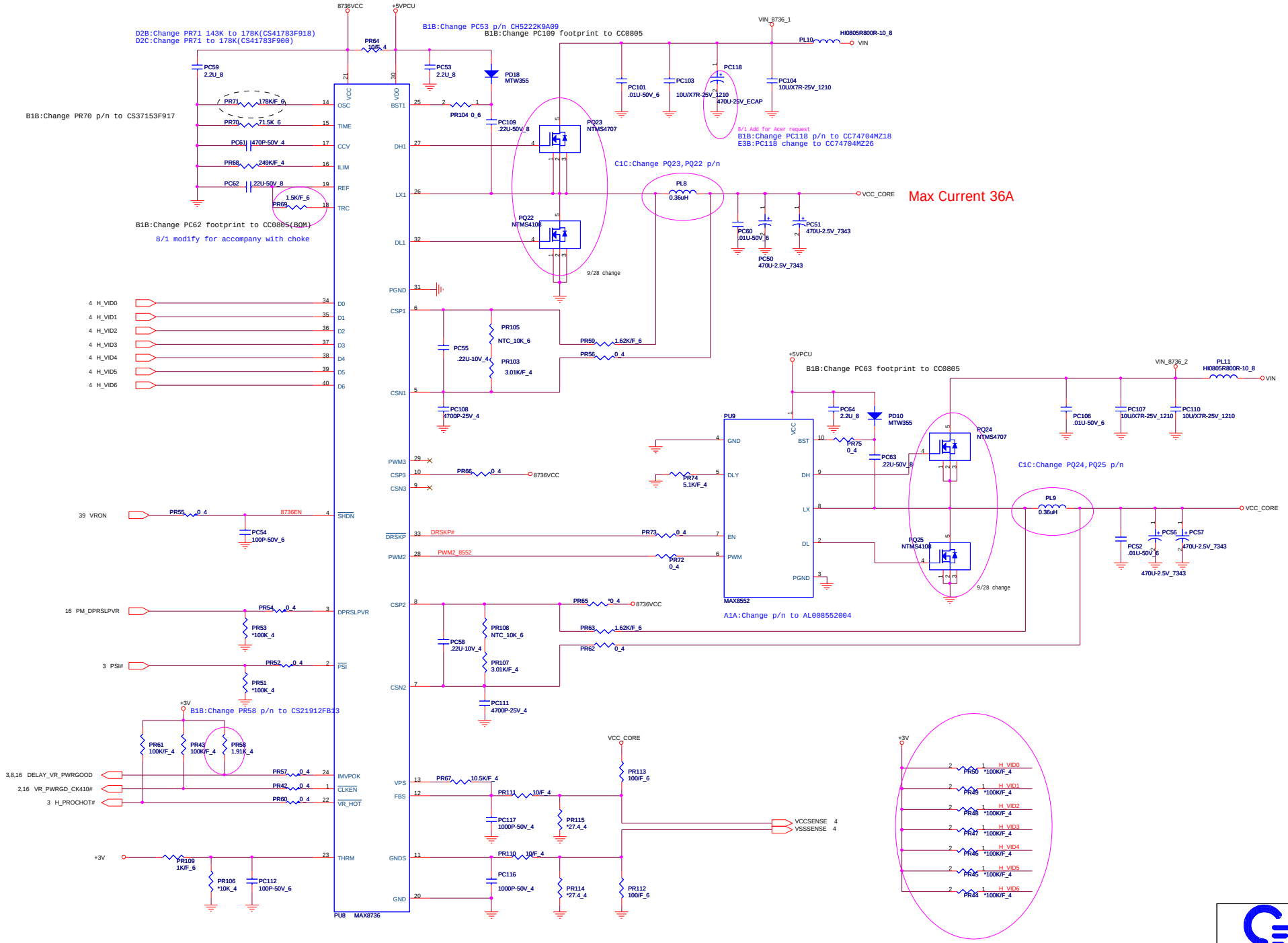

PROJECT : ZC1

Quanta Computer Inc.

Size	Document Number	Rev
	VCORE (MAX8736)	1A

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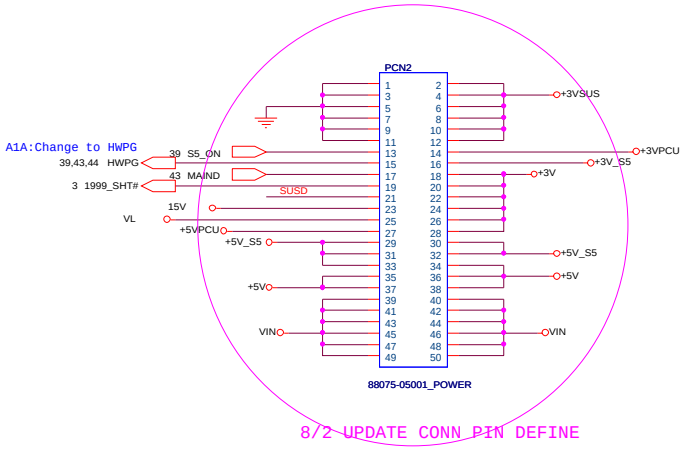

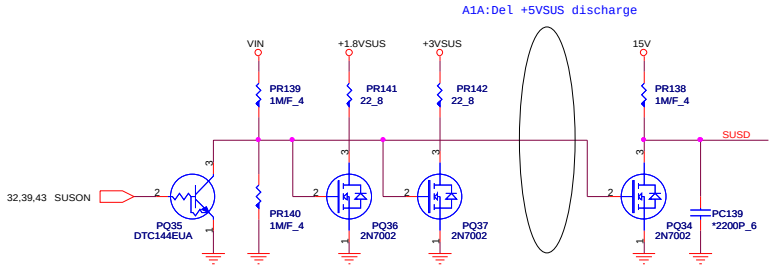

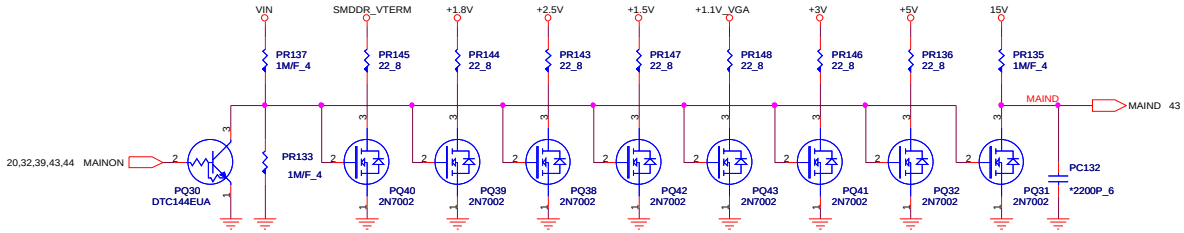

PROJECT : ZC1

Quanta Computer Inc.

Size	Document Number	Rev
	DISCHARGE/CONNECTOR	1A

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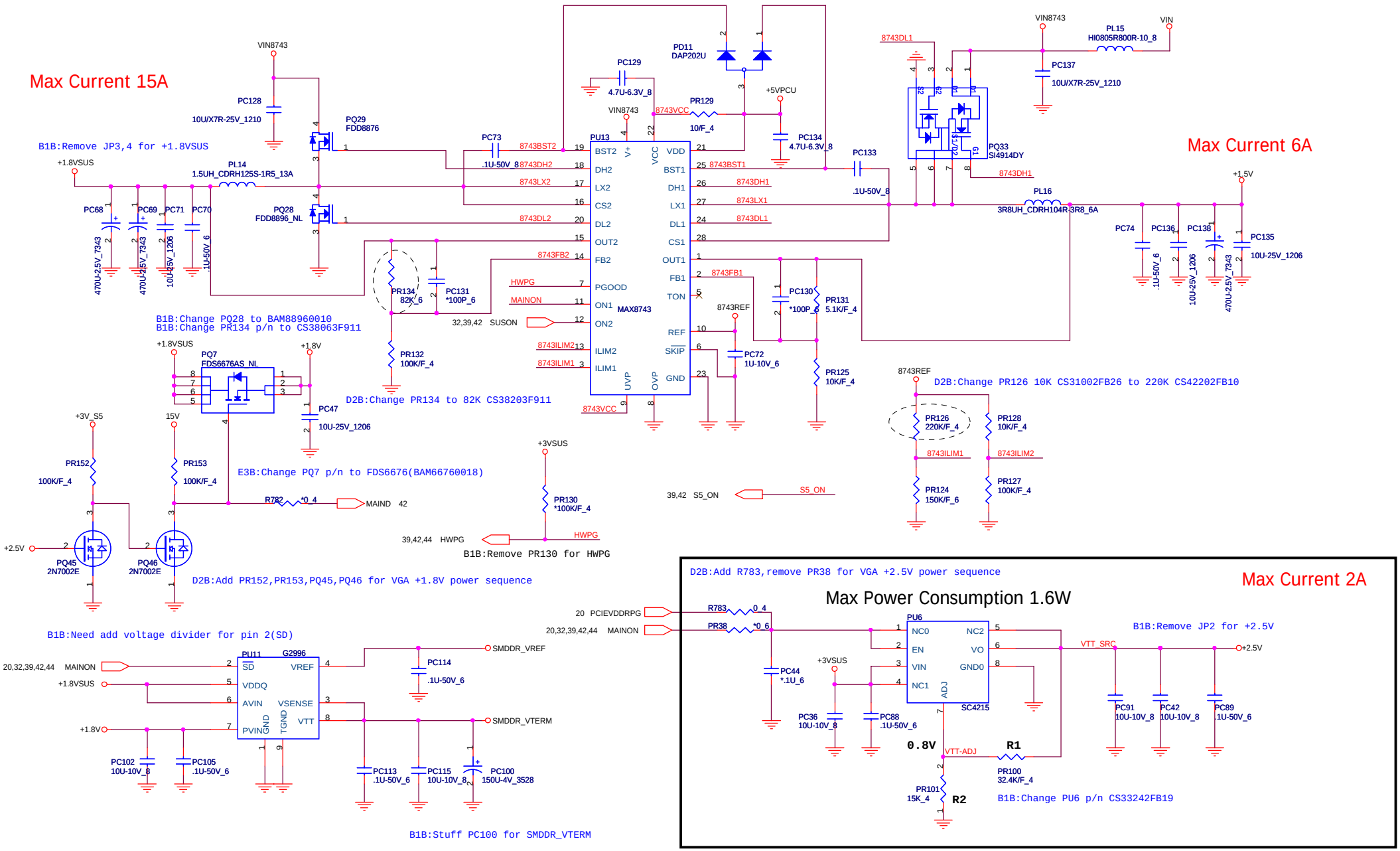
Max Current 15A
Max Current 6A
Max Current 2A
Max Power Consumption 1.6W
B1B:Remove JP3,4 for +1.8VSUS
B1B:Change PQ28 to BAM88960010
B1B:Change PR134 p/n to CS38063F911
D2B:Change PR134 to 82K CS38203F911
E3B:Change PQ7 p/n to FDS6676(BAM66760018)
D2B:Add PR152,PR153,PQ45,PQ46 for VGA +1.8V power sequence
B1B:Need add voltage divider for pin 2(SD)
B1B:Stuff PC100 for SMDDR_VTERM
B1B:Remove PR130 for HWPG
D2B:Change PR126 10K CS31002FB26 to 220K CS42202FB10
D2B:Add R783,remove PR38 for VGA +2.5V power sequence
B1B:Remove JP2 for +2.5V
B1B:Change PU6 p/n CS33242FB19
MAX8743
G2996
SC4215
PQ33 SI4914DY
PQ7 FDS6676AS_NL
PQ28 FDD8896_NL
PQ29 FDD8876
PQ45 2N7002E
PQ46 2N7002E
PL14 1.5UH_CDRH125S-1R5_13A
PL15 HI0805R800R-10_8
PL16 3R8UH_CDRH104R-3R8_6
PD11 DAP202U
VIN8743
VIN
+1.8VSUS
+1.5V
+5VPCU
+3V_S5
+3VSUS
+2.5V
+1.8V
15V
SMDDR_VREF
SMDDR_VTERM
VTT_SRC
VTT-ADJ
0.8V
R1
R2
20 PCIEVDDRPG
20,32,39,42,44 MAINON
32,39,42 SUSON
39,42 S5_ON
39,42,44 HWPG
MAIND 42
PROJECT : ZC1
Quanta Computer Inc.
Size
Document Number
+2.5V/+1.8VSUS / +1.5V
Rev
A
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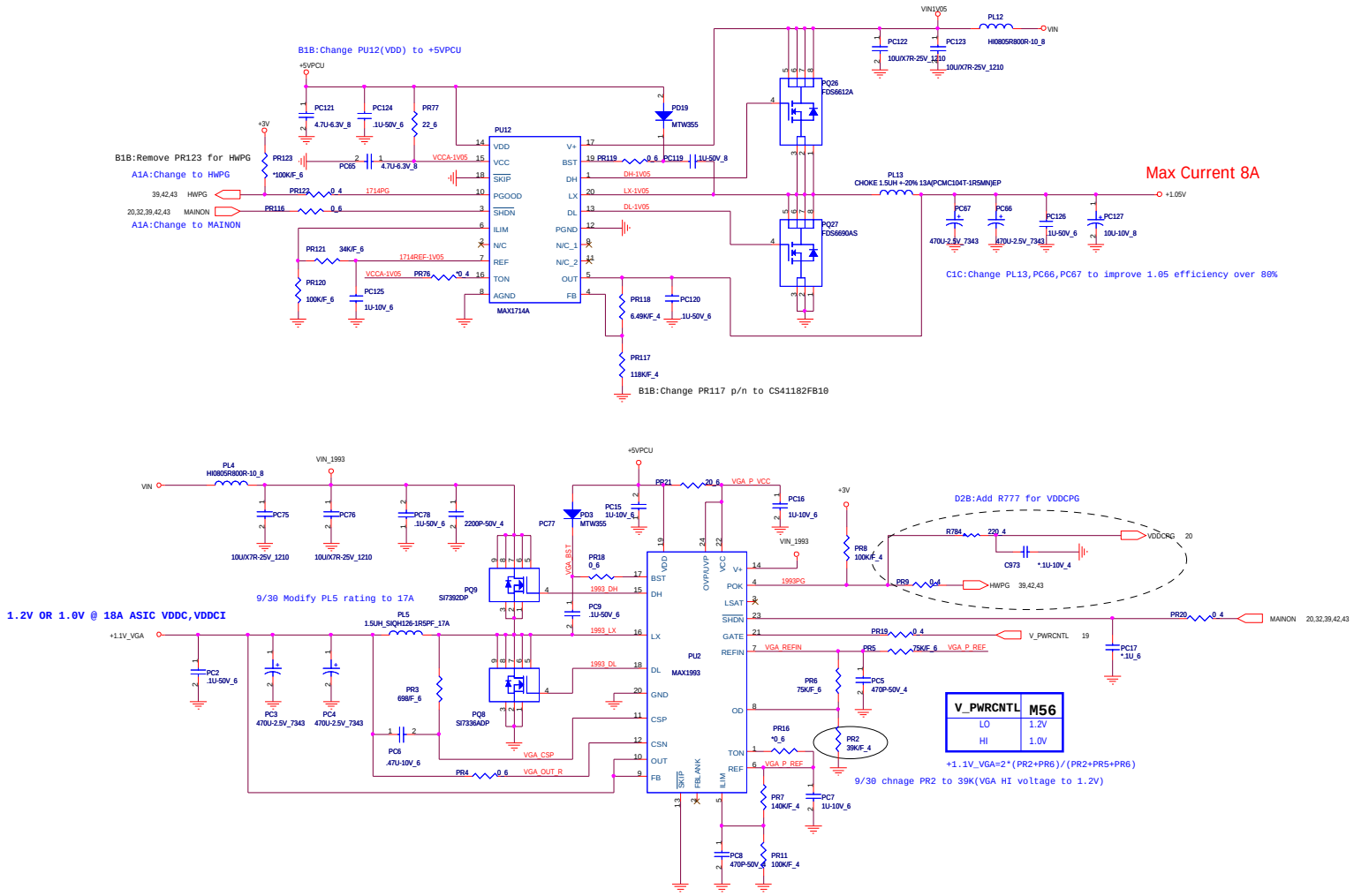

V_PWRCNTL	M56
LO	1.2V
HI	1.0V

B1B:Change PR39 p/n to CS32003F933

D2B:Remove PR39,PR40,PR41,PC46,PC48,PC49,PC98,PC99,PU7 for +1.2V_VPCIE

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Quanta Computer Inc.

Size	Document Number	Rev
Custom	+1.05V/+1.2V_VGA/+1.2V	1A

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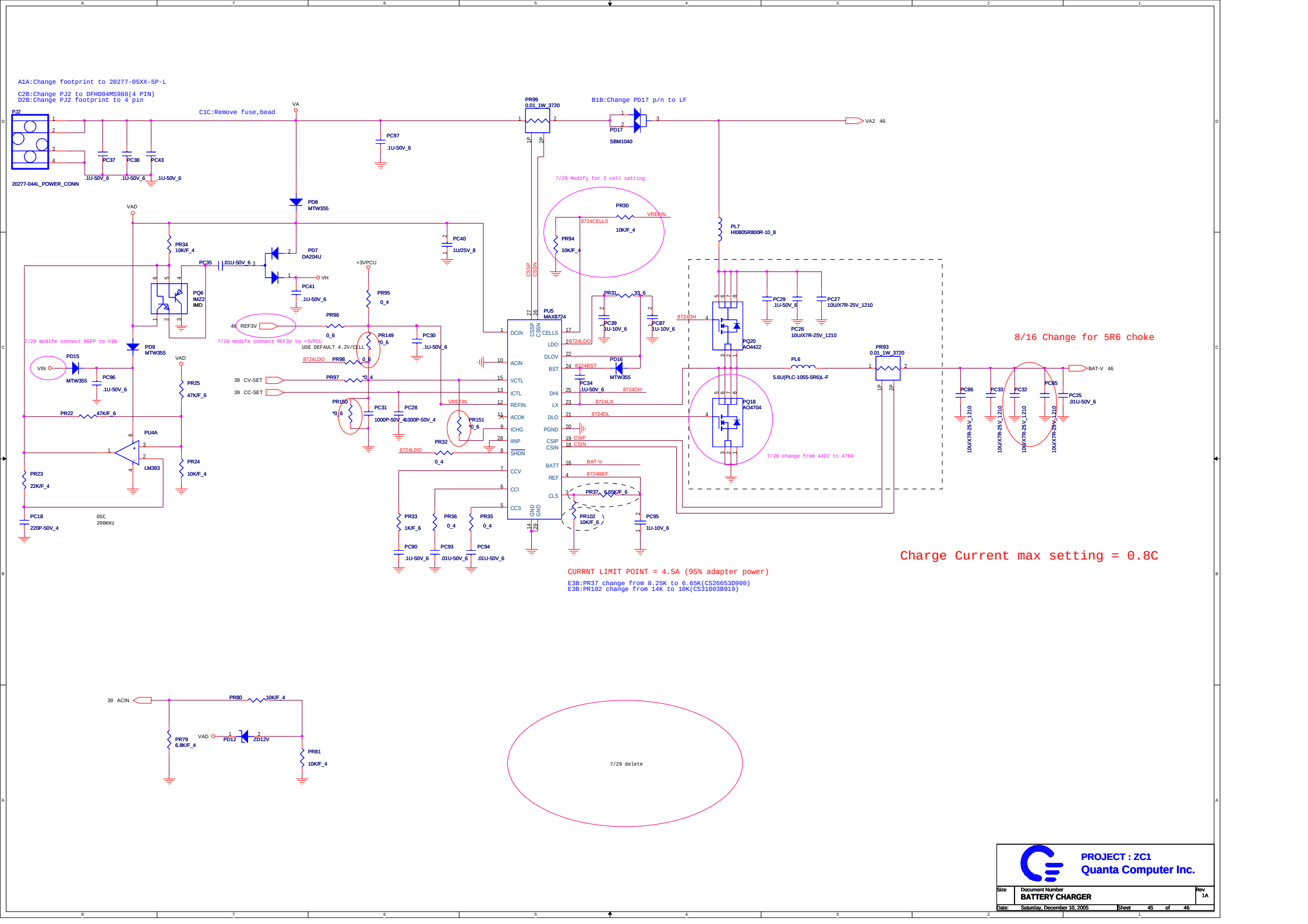
A1A:Change footprint to 20277-05XX-5P-L
C2B:Change PJ2 to DFHD04MS988(4 PIN)
D2B:Change PJ2 footprint to 4 pin
C1C:Remove fuse,bead
B1B:Change PD17 p/n to LF
PJ2
20277-044L_POWER_CONN
PC37 .1U-50V_6
PC38 .1U-50V_6
PC43 .1U-50V_6
VA
PC97 .1U-50V_6
PR99 0.01_1W_3720
PD17 SBM1040
VA2 46
PD8 MTW355
VAD
PR34 10K/F_4
PC35 .01U-50V_6
PD7 DA204U
VH
PC41 .1U-50V_6
PC40 1U/25V_8
+3VPCU
PQ6 IMZ2 IMD
PR95 0_4
PR96 0_6
46 REF3V
7/29 modife connect REFP to VIN
7/29 modife connect REF3V to +3VPCU
USE DEFAULT 4.2V/CELL
PR149 *0_6
PC30 .1U-50V_6
PD9 MTW355
PD15 MTW355
VIN
PC96 .1U-50V_6
8724LDO PR98 0_6
39 CV-SET
39 CC-SET
PR97 *0_4
PR25 47K/F_6
PR22 47K/F_6
PR180 *0_6
PC31 1000P-50V_4
PC28 1000P-50V_4
VREFIN
PR151 *0_6
PU4A LM393
PR24 10K/F_4
PR23 22K/F_4
PR32 0_4
8724LDO
PC18 220P-50V_4
OSC 200KHz
PR33 1K/F_6
PR36 0_4
PR35 0_4
PC90 .1U-50V_6
PC93 .01U-50V_6
PC94 .01U-50V_6
7/29 Modify for 3 cell setting
PR30 10K/F_4
8724CELLS
VREFIN
PR94 10K/F_4
CSSP
CSSN
PU5 MAX8724
DCIN
ACIN
VCTL
ICTL
REFIN
ACOK
ICHG
IINP
SHDN
CCV
CCI
CCS
CELLS
LDO
DLOV
BST
DHI
LX
DLO
PGND
CSIP
CSIN
BATT
REF
CLS
GND
8724LDO
PR31 33_6
PC39 1U-10V_6
PC87 1U-10V_6
PD16 MTW355
PC34 1U-50V_6
8724BST
8724DH
8724LX
8724DL
CSIP
CSIN
BAT-V
8724REF
PR37 6.65K/F_6
PR102 10K/F_6
PC95 1U-10V_6
PL7 HI0805R800R-10_8
PC29 .1U-50V_6
PC27 10U/X7R-25V_1210
PC26 10U/X7R-25V_1210
PQ20 AO4422
PQ18 AO4704
7/29 change from 4422 to 4704
PL6 5.6U(PLC-1055-5R6)L-F
PR93 0.01_1W_3720
8/16 Change for 5R6 choke
PC86 10U/X7R-25V_1210
PC33 10U/X7R-25V_1210
PC32 10U/X7R-25V_1210
PC85 10U/X7R-25V_1210
PC25 .01U-50V_6
BAT-V 46
Charge Current max setting = 0.8C
CURRNT LIMIT POINT = 4.5A (95% adapter power)
E3B:PR37 change from 8.25K to 6.65K(CS26653D900)
E3B:PR102 change from 14K to 10K(CS31003B919)
39 ACIN
PR80 10K/F_4
PR79 6.8K/F_4
VAD
PD12 ZD12V
PR81 10K/F_4
7/29 delete
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Quanta Computer Inc.
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BATTERY CHARGER
Rev 1A
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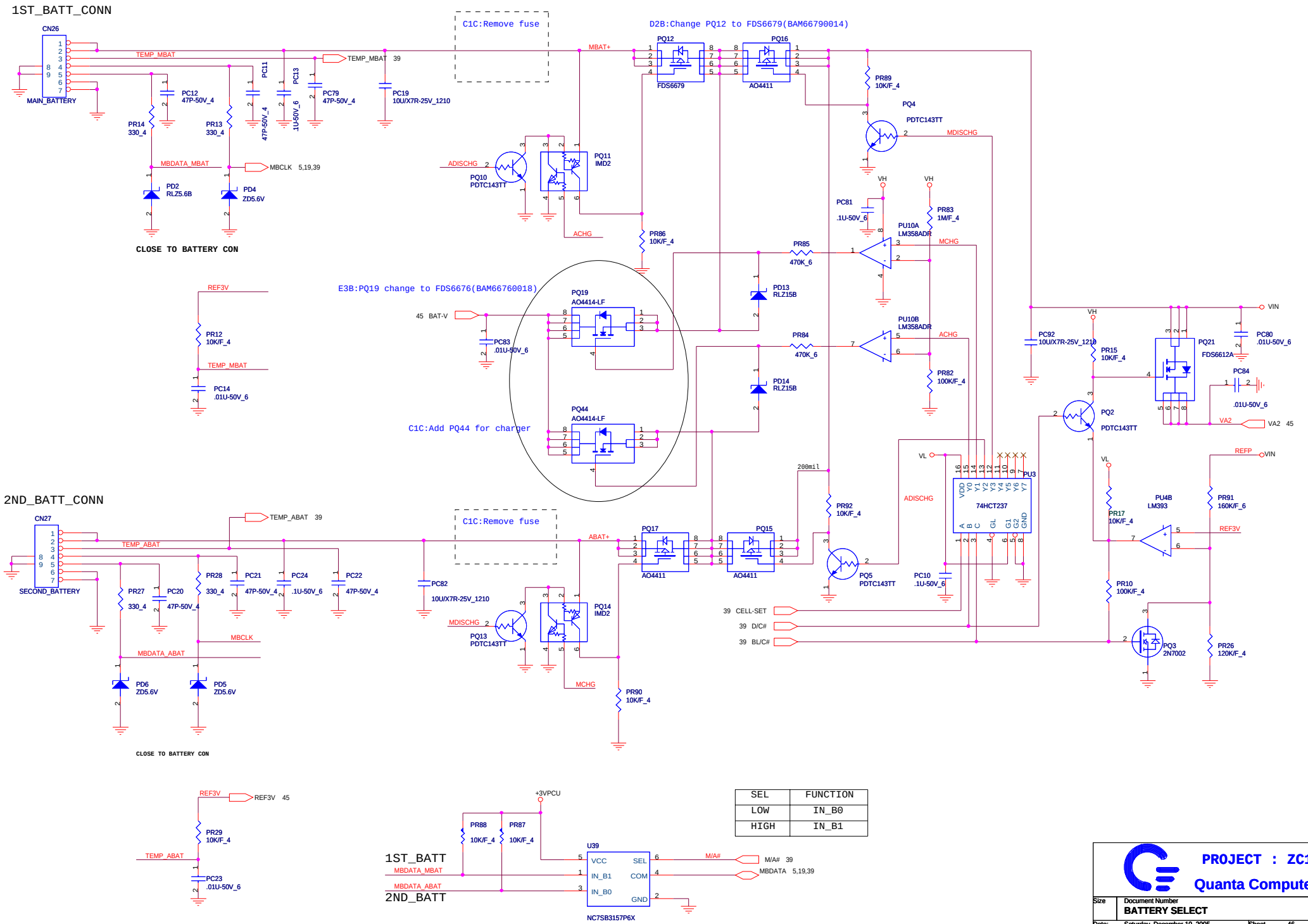
A1A:Change p/n to DFHD07MR391
B1B:Change CN26 footprint to 20175A-07G1-7P-R



SEL	FUNCTION
LOW	IN_B0
HIGH	IN_B1

PROJECT : ZC1

Quanta Computer Inc.

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	BATTERY SELECT	A

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